Time-Dependent Dielectric Breakdown-Reliability Characterization and Analysis of Advanced CMOS Devices

ASIFA AMIN

DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY DELHI

June, 2025

Time-Dependent Dielectric Breakdown-Reliability Characterization and Analysis of Advanced CMOS Devices

by

Asifa Amin

Department of Electrical Engineering

Submitted

in the fulfillment of the requirements of the degree of Doctor of Philosophy

to the

INDIAN INSTITUTE OF TECHNOLOGY DELHI

NEW DELHI - 110016, INDIA

June 2025

Dedicated
to
My Family

Certificate

This is to certify that the thesis entitled, **" Time-Dependent Dielectric Breakdown-Reliability Characterization and Analysis of Advanced CMOS Devices** ", being submitted by **Ms. Asifa Amin** to the Indian Institute of Technology Delhi, is worthy of consideration for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering and is a record of the original bonafide research work carried out by her. The results presented in the thesis have not been submitted in part or full, to any other University or Institute for the award of any degree or diploma.

I certify that she has pursued the prescribed course of research.

Date:

Place:

Prof. Abhisek Dixit
Professor,
Department of Electrical Engineering
Indian Institute of Technology Delhi
Hauz Khas, New Delhi – 110016

ACKNOWLEDGEMENTS

First and foremost, I would like to express my deepest gratitude to the Almighty for giving me the strength, patience, and perseverance to complete this journey. Without his blessings, none of this would have been possible.

I am profoundly grateful to my supervisor, Prof. Abhisek Dixit, for his exceptional guidance, encouragement, and mentorship throughout my PhD journey. His expertise and unwavering support have been pivotal in shaping my research skills and have influenced my personal development. Prof. Dixit's belief in my potential has not only refined my abilities as a researcher but has also fostered my growth as an individual. The wisdom and lessons imparted under his supervision will resonate with me and guide me throughout my life. Should I have the opportunity to work as a faculty member in the future, I aspire to embody the same qualities and commitment that Prof. Dixit exemplified as my mentor. I would also like to extend my sincere thanks to my Ph.D research Committee, Prof. Mukul Sarkar, Prof. Dhiman Malik, and Prof. Ankur Gupta for their valuable feedback, guidance, and support throughout my research. Their suggestions and expertise have been crucial to the successful completion of this work.

I would also like to express my heartfelt gratitude to our industry collaborators, Dr. Purushothaman Srinivasan and Dr. Oscar H. Gonzalez from GlobalFoundries for their consistent support and invaluable contributions to my research. Their suggestions and encouragement have significantly contributed to the success of this work. I am deeply grateful for their expertise and dedication.

I thank the Indian Institute of Technology Delhi, New Delhi, India, for providing all the facilities for my research activities. I gratefully acknowledge the Department of Science and Technology, Government of India, for providing me with the research Fellowship under the Innovation in Science Pursuit for Inspired Research (INSPIRE) scheme for my higher study.

I also wish to acknowledge my labmates, who have become like an extended family to me—Aarti Rathi, Sumreti Gupta, Shivendra Singh Rathur, Shruti Pathak, Sujit Singh,

Deepesh Sharma, Anuj Bhardwaj, Amit Sarkar, Parag, Smriti Shukla, Pulak, and Devendra Singh. They have provided me with a supportive and joyful environment, making the lab feel like a second home. They are cherished friends who have made the long hours in the lab not only bearable but also enjoyable. I deeply value the moments we've shared, both in our academic endeavors and personal interactions. I would also like to extend a heartfelt special mention to my dear friends, Iram, Nadeem, and Omais, whose support and companionship transformed my challenging early days at IIT-D into a journey of resilience and hope. Their encouragement and presence were instrumental in helping me persevere through difficulties, and without them, continuing my PhD journey would have been immensely harder.

To my family, to whom I will be eternally indebted, especially my father, Mohd. Amin Rather, my mother, Sharifa Banoo, my brother, Ishfaq Amin, my beloved sister, Farhana Amin, my sister-in-law, Rabiya, and my precious niece, Fajr, and nephew, Adeen—their love and support have been the cornerstone of my journey. They have been my refuge and my strength, providing a sense of balance and perspective when I needed it most. Their constant encouragement and belief in me have been a source of immense comfort and inspiration. I am profoundly grateful for their presence in my life and the countless ways they have supported me. I am thankful to my little sisters, Hadeeqa and Aisha, whose admiration and belief in me have been a constant source of motivation, inspiring me to work harder and strive for excellence. A special thanks goes to my husband, Aamir Ul Islam, who has been my steadfast pillar of strength. Since the beginning of our journey together, he has continuously encouraged me to chase my dreams and has supported me unconditionally through every challenge. His selfless love, patience, and belief in me have been the bedrock of this journey. I am very grateful for his enduring support and the countless ways he has been there for me. A heartfelt thanks to my in-laws for their warmth, love, and understanding. Their support has been invaluable in helping me pursue my dream.

At last, I sincerely thank all who have supported me, directly or indirectly, throughout my PhD journey. Your encouragement and help mean so much to me.

Asifa Amin

ABSTRACT

The continuous scaling of semiconductor devices to meet the increasing need for high-speed processing and greater integration levels has introduced critical reliability challenges that include Time-Dependent Dielectric Breakdown (TDDB), Bias Temperature Instability (BTI), Hot Carrier Degradation (HCD), and Electromigration (EM). Among these, TDDB has always emerged as one of the significant issues, particularly in advanced CMOS technologies. As the industry moves towards novel applications such as quantum computing, millimeter-wave (mm-wave) communications, and low-power digital circuits, understanding and addressing TDDB concerns across these diverse technology spaces is of utmost importance. The increasing power dissipation in these applications further necessitates the study of reliability at elevated temperatures, where device lifetime and performance are adversely affected. Therefore, both DC and AC TDDB analysis at high temperatures is critical for enhancing reliability predictions and improving device design.

In this thesis, an extensive experimental investigation of TDDB in 45nm RFSOI-based MOSFETs is conducted under DC, AC, and RF stress conditions. This study systematically explores the influence of key parameters, such as device layout, operating temperature, and stress characterization techniques, on dielectric breakdown. The generation of defects, including oxide and interface traps, is examined to provide a deeper understanding of breakdown mechanisms. A detailed analysis of the relationship between device geometry—specifically the gate area-to-perimeter ratio—and TDDB is performed on both DC and RF FETs fabricated using 45nm RFSOI technology. The results reveal significant deviations from the power-area scaling law and underscore the need for critical reassessment of reliability models in advanced technology nodes.

Furthermore, for the first time, this thesis investigates TDDB behavior at cryogenic temperatures in MOSFETs used in quantum computing control circuits. The results demonstrate that the characteristic breakdown time (t63) tends to increase with decreasing temperature, exhibiting a minor saturation effect at cryogenic temperatures.

Additionally, the Weibull slope (β) exhibits an inverted U-shaped dependence on temperature, with its maximum observed between 100K and 200K across all voltage levels. Both the trap generation rate and critical defect density are estimated, and the observed trends in β are interpreted in the context of multiple breakdown origins within the cryogenic temperature range. These findings provide valuable insights for optimizing gate oxide thickness in cryogenic CMOS circuits, crucial for future quantum applications.

In addition, this thesis presents a comprehensive experimental study on AC-TDDB in 45nm PDSOI-based MOSFETs with varying gate oxide thicknesses and polarities. The lifetime of devices under AC stress conditions, including frequencies up to 1 GHz and varying duty cycles, is predicted using the frequency power law. A significant 90X increase in t63 is observed at RF frequencies compared to DC stress in thin NFETs. This investigation, performed using SILC spectroscopy, reveals that the breakdown behavior and trap generation rate are functions of frequency, duty cycle, and gate sense voltage. These findings enhance our understanding of dielectric reliability under AC stress and enable more accurate lifetime predictions for digital circuits.

Finally, the mechanisms of TDDB in RF devices are explored under both DC and RF stress in 45nm RFSOI technology. The analysis shows that RF devices exhibit a reduced lifespan under combined DC and RF stress, with an inverse correlation between t63 and input power (P_{in}) at millimeter-wave frequencies. The impact of peak voltage (V_{Peak}) on device lifetime is also modeled, providing further insights into the degradation mechanisms at high input powers. This research lays a strong foundation for future advancements in RF TDDB reliability, offering crucial insights for both RF device applications and the design of next-generation high-frequency circuits.

This comprehensive work bridges the gap between fundamental TDDB analysis and practical applications in advanced technology nodes, offering significant contributions to the fields of semiconductor reliability, cryogenic CMOS, and RF device design.

सार

सेमीकंडक्टर डिवाइसेज के लगातार स्केलिंग ने, उच्च गति प्रसंस्करण और एकीकरण की बढ़ती मांग को पूरा करने के लिए, टाइम-डिपेंडेंट डाइलेक्ट्रिक ब्रेकडाउन (TDDB), हॉट कैरियर डिग्रेडेशन (HCD), बायस टेम्परेचर इंस्टेबिलिटी (BTI), और इलेक्ट्रोमाइग्रेशन (EM) जैसे महत्वपूर्ण विश्वसनीयता चुनौतियाँ पेश की हैं। इनमें से, TDDB उन्नत CMOS तकनीकों में सबसे महत्वपूर्ण मुद्दों में से एक के रूप में उभरा है। जैसे-जैसे उद्योग क्वांटम कंप्यूटिंग, मिलीमीटर-वेव (mm-wave) संचार और लो-पावर डिजिटल सर्किट्स जैसे नए अनुप्रयोगों की ओर बढ़ रहा है, इन विभिन्न तकनीकी क्षेत्रों में TDDB के मुद्दों को समझना और हल करना अत्यंत महत्वपूर्ण हो गया है। इन अनुप्रयोगों में बढ़ती पावर डिसिपेशन भी उच्च तापमान पर विश्वसनीयता के अध्ययन की आवश्यकता को बढ़ाती है, जहां डिवाइस की जीवनकाल और प्रदर्शन पर नकारात्मक प्रभाव पड़ता है। इसलिए, उच्च तापमान पर DC और AC TDDB विश्लेषण विश्वसनीयता भविष्यवाणियों को बढ़ाने और डिवाइस डिज़ाइन को बेहतर बनाने के लिए महत्वपूर्ण है।

इस थीसिस में, 45nm RFSOI-आधारित MOSFETs में DC, AC, और RF तनाव स्थितियों के तहत TDDB का व्यापक प्रायोगिक अध्ययन किया गया है। यह अध्ययन डाइलेक्ट्रिक ब्रेकडाउन पर डिवाइस लेआउट, ऑपरेटिंग तापमान और तनाव वर्णन तकनीकों जैसे प्रमुख मानकों के प्रभाव को व्यवस्थित रूप से अन्वेषण करता है। डिफेक्ट्स की उत्पत्ति, जिनमें ऑक्साइड और इंटरफ़ेस ट्रैप्स शामिल हैं, का विश्लेषण किया गया है ताकि ब्रेकडाउन तंत्रों को गहराई से समझा जा सके। डिवाइस ज्यामिति—विशेष रूप से गेट क्षेत्र-से-पेरिमीटर अनुपात—और TDDB के बीच संबंध का विस्तृत विश्लेषण DC और RF FETs दोनों पर किया गया है, जिन्हें 45nm RFSOI तकनीक का उपयोग करके निर्मित किया गया है। परिणाम पावर-एरिया स्केलिंग लॉ से महत्वपूर्ण विचलन दर्शाते हैं और उन्नत तकनीकी नोड्स में विश्वसनीयता मॉडलों की महत्वपूर्ण पुन: जाँच की आवश्यकता पर जोर देते हैं।

इसके अलावा, इस थीसिस में पहली बार, क्वांटम कंप्यूटिंग कंट्रोल सर्किट्स में उपयोग किए गए MOSFETs में क्रायोजेनिक तापमान पर TDDB व्यवहार की जांच की गई है। परिणाम बताते हैं कि तापमान कम होने पर विशिष्ट ब्रेकडाउन समय (t63) बढ़ता है, और अल्ट्रा-लो तापमान पर एक कमजोर संतृप्ति प्रभाव देखा गया है। सभी वोल्टेज रेंज में वेइबुल स्लोप (β) एक उल्टे U-आकार का व्यवहार प्रदर्शित करता है, जिसमें 100K और 200K के बीच एक शिखर देखा गया है। ट्रैप उत्पादन दर और महत्वपूर्ण दोष घनत्व का अनुमान लगाया गया है, और β में देखे गए रुझानों को क्रायोजेनिक तापमान रेंज में एकाधिक ब्रेकडाउन उत्पत्तियों के संदर्भ में व्याख्या की गई है। ये निष्कर्ष क्रायोजेनिक CMOS सर्किट्स में गेट ऑक्साइड की मोटाई को अनुकूलित करने के लिए मूल्यवान अंतर्दृष्टि प्रदान करते हैं, जो भविष्य के क्वांटम अनुप्रयोगों के लिए महत्वपूर्ण है।

इस थीसिस में 45nm PDSOI-आधारित MOSFETs में विभिन्न गेट ऑक्साइड मोटाई और ध्रुवीयताओं के साथ AC-TDDB पर एक व्यापक प्रायोगिक अध्ययन भी प्रस्तुत किया गया है। AC तनाव स्थितियों के तहत डिवाइसेज के जीवनकाल का पूर्वानुमान, जिसमें 1 GHz तक की आवृत्तियाँ और विभिन्न ड्यूटी साइकल्स शामिल हैं, आवृत्ति पावर लॉ का उपयोग करके किया गया है। पतले NFETs में DC तनाव की तुलना में RF आवृत्तियों पर t63 में 90X की महत्वपूर्ण वृद्धि देखी गई है। यह जांच, जो SILC स्पेक्ट्रोस्कोपी का उपयोग करके की गई है, बताती है कि ब्रेकडाउन व्यवहार और ट्रैप उत्पादन दर आवृत्ति, ड्यूटी साइकल, और गेट सेंस वोल्टेज के कार्य होते हैं। ये निष्कर्ष AC तनाव के तहत डाइलेक्ट्रिक विश्वसनीयता की हमारी समझ को बढ़ाते हैं और डिजिटल सर्किट्स के लिए अधिक सटीक जीवनकाल भविष्यवाणियों को सक्षम करते हैं।

अंत में, 45nm RFSOI तकनीक में DC और RF तनाव के तहत RF डिवाइसेज में TDDB के तंत्रों की जांच की गई है। विश्लेषण से पता चलता है कि RF डिवाइसेज DC और RF तनाव के संयोजन के तहत कम जीवनकाल प्रदर्शित करते हैं, जिसमें मिलीमीटर-वेव आवृत्तियों पर t63 और इनपुट पावर (P_{in}) के बीच एक विपरीत संबंध होता है। डिवाइस जीवनकाल पर पीक वोल्टेज (V_{Peak}) के प्रभाव को भी मॉडल किया गया है, जो उच्च इनपुट पावर पर गिरावट तंत्रों में और अंतर्दृष्टि प्रदान करता है। यह शोध RF TDDB विश्वसनीयता में भविष्य के प्रगति के लिए एक मजबूत नींव रखता है, जो RF डिवाइस अनुप्रयोगों और अगली पीढ़ी के उच्च आवृत्ति सर्किट्स के डिज़ाइन के लिए महत्वपूर्ण अंतर्दृष्टियाँ प्रदान करता है।

यह व्यापक कार्य मौलिक TDDB विश्लेषण और उन्नत तकनीकी नोड्स में व्यावहारिक अनुप्रयोगों के बीच की खाई को पाटता है, सेमीकंडक्टर विश्वसनीयता, क्रायोजेनिक CMOS, और RF डिवाइस डिज़ाइन के क्षेत्रों में महत्वपूर्ण योगदान प्रदान करता है।

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

Abbreviation	Description
AC	Alternating Current
AHI	Anode Hole Injection
AHR	Anode Hydrogen Release
BTI	Bias Temperature Instability
CCR	Closed Cycle Refrigeration
CMOS	Complementary Metal Oxide Semiconductor
CVS	Constant Voltage Stress
CW	Continuous Wave
DC	Direct Current
DUT	Device under Test
EOT	Equivalent Oxide Thickness
FET	Field Effect Transistor
GSG	Ground Signal Ground
HCD	Hot Carrier Degradation
IC	Integrated Circuit
LNA	Low Noise Amplifier
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PA	Power Amplifier
PDSOI	Partially Depleted Silicon-On-Insulator
RF	Radio Frequency
RSU	Remote Sense and Switching Unit

SCE	Short Channel Effect
SMU	Source Measure Unit
SOC	System On Chip
SOI	Silicon On Insulator
SOLT	Short Open Load Thru
TDDB	Time-Dependent Dielectric Breakdown
TMP	Turbo Molecular Pump
TRL	Thru Reflect Load
TTF	Time To Fail
VBD	Breakdown Voltage
VNA	Vector Network Analyzer
WGFMU	Waveform Generator Fast Measurement Unit