

**DESIGN AND ANALYSIS OF
EMERGING NANOSCALE
JUNCTIONLESS FETS FROM GATE-
INDUCED DRAIN LEAKAGE
PERSPECTIVE**

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by

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Dedicated to

Dada ji, Dadi Maa, Mumma, Papa, Saumya and all the teachers whom I came across at different stages during the last 24 years of my life. Some motivated me, some inspired me, some helped in designing the process flow of my life, often poking me with a sharp stick called “truth”, enabling my fabrication in the present form.

कर्मण्येवाधिकारस्ते मा फलेषु कदाचन।
मा कर्मफलहेतुर्भूर्मा ते सङ्गोऽस्त्वकर्मणि ॥ २-४७

- *Shrimad Bhagwad Gita, Chapter 2, Verse: 47*

हिन्दी: कर्म करो फल की चिंता मत करो ।

English: *You have the right to work only.*

*Do not let the expected outcome of your action be your motive, nor
let yourself attach to inaction.*

Certificate

This is to certify that the thesis entitled “*Design and Analysis of Emerging Nanoscale Junctionless FETs from Gate-Induced Drain Leakage Perspective*” being submitted by **Mr. Shubham Sahay** for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under my supervision and guidance. The matter embodied in this thesis has not been submitted for the award of any other degree or diploma.

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Abstract

CMOS scaling has been the driving machinery behind this era of internet of things (IoT) and big data. However, CMOS scaling has reached its bottleneck owing to the significant power dissipation. The incessant scaling of the MOSFETs has increased the OFF-state leakage current significantly resulting in significantly high static power dissipation. Although scaling the power supply may reduce the static power dissipation, it degrades the ON-state to OFF-state current ratio because of the Boltzmann tyranny of 60mV/decade sub-threshold swing in the conventional MOSFETs which arises due to the inherent thermionic conduction mechanism.

Two probable solutions have been proposed to overcome this CMOS scaling bottleneck: (a) alternate device architectures with improved electrostatic gate control like finFETs, gate-all-around nanowire (GAA NW) (b) alternate conduction mechanism i.e. band-to-band-tunneling or impact ionization based steep sub-threshold swing devices such as Tunnel FETs (TFETs) and impact ionization MOS (IMOS).

Although GAA NWFETs offer the best possible gate control leading to suppression of the short channel effects, unfortunately, the efficient gate control results in a considerable band overlap of the valence band of the channel region with the conduction band of the drain region. This facilitates a band-to-band-tunneling (BTBT) of electrons from channel to the drain increasing the OFF-state leakage current significantly. This new component of gate-induced drain leakage (GIDL) known as lateral BTBT (L-BTBT) is unique to the NWFETs and hinders their scaling.

Furthermore, scaling the MOSFETs to the sub-10 nm regime requires ultra-steep doping profiles at the metallurgical junctions. However, realising such an ultra-steep doping profile is extremely difficult. Therefore, FETs without any metallurgical junctions known as junctionless FETs (JLFETs) were proposed. However, the GIDL in JLFETs leads to the formation of a parasitic bipolar junction transistor (BJT) which is triggered in the OFF-state leading to a significantly high leakage current.

Therefore, this thesis addresses this important issue of GIDL in emerging nano-scale FETs which increases the OFF-state leakage current in NWFETs and JLFETs. First, a physical insight into the nature of GIDL in different NWFET configurations is

provided. A parasitic BJT theory is proposed to explain the difference in the nature of NWJLFETs and NWMOSFETs. The diameter dependent dominant leakage mechanisms in the NWJLFETs are then analysed. The spacer design guidelines for: (a) NWFETs without source/drain extension underlap and (b) NWFETs with source/drain extension underlap are provided from a GIDL perspective.

Furthermore, a NWFET with a dual metal stacked gate architecture (DMSG) is proposed to mitigate the GIDL and efficiently scale the NWFETs to the sub-10 nm regime. A comprehensive analysis of GIDL in the recently reported nanotube (NT) FETs which are essentially NWFETs with a core gate is performed. A NTJLFET is also proposed to suppress the GIDL i.e. BTBT induced parasitic BJT action. A core-shell NWJLFET with a p^+ -core is proposed to (a) mitigate the BTBT induced parasitic BJT action in NWJLFETs with nanowire diameter < 10 nm and (b) realize efficient volume depletion in NWJLFETs with nanowire diameter > 10 nm.

The efficacy of the dual-material gate (DMG) architecture to mitigate the GIDL in NWJAMFETs is also analysed for the first time. An extended back gate architecture for scaling the double gate (DG) JLFETs to the sub-10 nm regime by diminishing the GIDL is proposed. In addition, a SOI JLFET with a hole sink layer to suppress the parasitic BJT action GIDL is presented. Buried oxide (BOX) engineering i.e. inclusion of a high- κ BOX to realize efficient volume depletion is also proposed for SOI JLFETs.

सार

CMOS स्केलिंग (IOT) और बड़े डेटा के इस युग के पीछे ड्राइविंग मशीन रही है। हालांकि, महत्वपूर्ण बिजली अपव्यय के कारण CMOS स्केलिंग अपने bottleneck पर पहुंच गया है। MOSFET के निरंतर स्केलिंग में ऑफ-स्टेट रिसाव की बढ़ोतरी में वृद्धि हुई है जिससे महत्वपूर्ण रूप से उच्च स्थैतिक पावर अपव्यय में वृद्धि हुई है। यद्यपि बिजली की आपूर्ति को स्केलिंग स्थिर शक्ति अपव्यय को कम कर सकती है, यह MOSFET को ON-OFF-स्टेट चालू अनुपात को घटाता है क्योंकि पारंपरिक MOSFET में 60 mV / दशक के sub-threshold स्विंग के बॉटलनेक tyranny की वजह से थर्मोनिक चालन तंत्र के कारण उत्पन्न होता है।

CMOS स्केलिंग बाधाओं से उबरने के लिए दो संभावित समाधान प्रस्तावित किए गए हैं: (ए) बेहतर इलेक्ट्रोस्टैटिक गेट नियंत्रण जैसे FinFETs, गेट-ऑल-नैनोवायर (GAA NW) (बी) वैकल्पिक प्रवाहकत्व तंत्र यानी बैंड-टू-बैंड- टनल FET (TFET) और प्रभाव आयनाईकरण MOS (IMOS) जैसे सुरंग या प्रभाव आयनकरण आधारित खड़ी sub-threshold स्विंग डिवाइस। हालांकि, GAA NWFETs सबसे अच्छा संभव गेट नियंत्रण की पेशकश करते हैं जो कि छोटे चैनल प्रभावों को दमन करने के लिए अग्रणी होता है, दुर्भाग्य से, कुशल गेट नियंत्रण परिणाम, drain क्षेत्र के conduction बैंड के साथ चैनल क्षेत्र के valence बैंड के काफी बैंड ओवरलैप में होता है। यह चैनल से बैंड-टू-बैंड-टनलिंग (BTBT) की सुविधा देता है जिससे ऑफ-स्टेट रिसाव चालू होने से नाले में बढ़ोतरी हो सकती है। पार्श्व बीटीबीटी (L-BTBT) के रूप में जाना गेट से प्रेरित drain रिसाव (GIDL) का यह नया घटक NWFET के लिए अद्वितीय है और अपने स्केलिंग को बाधित करता है। इसके अलावा, MOSFET को उप 10-nm शासन में स्केलिंग करने के लिए धातुकर्म जंक्शनों पर अल्ट्रा-खड़ी डोपिंग प्रोफाइल की आवश्यकता होती है। हालांकि, इस तरह के अल्ट्रा-खड़ी डोपिंग प्रोफाइल का एहसास बेहद मुश्किल है। इसलिए, किसी भी धातुकर्म जंक्शन के बिना FET का प्रस्ताव किया गया था, जिसे Junctionless FET (JLFET) कहा जाता था। हालांकि, JLFET में GIDL एक परजीवी द्विध्रुवी जंक्शन ट्रांजिस्टर (BJT) के गठन की ओर अग्रसर है जो sub-20 nm में शुरू हो रहा है जिससे एक महत्वपूर्ण उच्च रिसाव चालू होता है।

इसलिए, इस थीसिस ने उभरते नैनो पैमाने के FET में GIDL के इस महत्वपूर्ण मुद्दे को संबोधित किया है जो NWFET और JLFET में ऑफ-स्टेट रिसाव को बढ़ाता है। सबसे पहले, विभिन्न NWFET कॉन्फिगरेशन में GIDL की प्रकृति में एक भौतिक अंतर्दृष्टि प्रदान की जाती है। NWJLFETs और NWMOSFETs की प्रकृति में अंतर को स्पष्ट करने के लिए एक परजीवी BJT सिद्धांत प्रस्तावित किया गया है। उसके बाद NWFET में व्यास पर निर्भर प्रभावी sरिसाव तंत्र का विश्लेषण किया जाता है। स्पेसर डिजाइन दिशानिर्देश निम्न के लिए: (ए) Source / drain विस्तार के बिना NWFET और (बी) Source / Drain विस्तार के साथ NWFET GIDL परिप्रेक्ष्य से उपलब्ध कराए जाते हैं।

इसके अलावा, NWFET, एक दोहरी धातु वाली गेट (DMSG) के साथ GIDL को कम करने और उप -10 एनएम शासन के कुशलता से NWFET को स्केल करने का प्रस्ताव है। हाल ही में नैनोव्यूब (NTFET) में GIDL का एक व्यापक विश्लेषण किया गया है जो मुख्य द्वार के साथ अनिवार्य रूप से NWFET हैं। NTJLFET को भी GIDL को दबाने का प्रस्ताव है, अर्थात् BTBT प्रेरित परजीवी बीजेटी कार्रवाई। P -कोर के साथ एक कोर-शंख NWJLFET प्रस्तावित है (ए) NWJLFET में नैनोवायर व्यास के साथ बीटीबीटी प्रेरित परजीवी बीजेटी कार्रवाई को कम कर देता है और (बी) NWJLFETs में nanowire व्यास के साथ > 10 एनएम पर्याप्त मात्रा में कमी महसूस करते हैं।

NWJLFET में GIDL को कम करने के लिए ड्यूल-मेटल gate (DMG) आर्किटेक्चर की प्रभावकारिता का भी पहली बार विश्लेषण किया गया है। GIDL को कम करके उप -10 एनएम शासन के लिए डबल गेट (DG) JLFET स्केलिंग के लिए एक विस्तारित बैक गेट वास्तुकला प्रस्तावित है। इसके अलावा, परजीवी बीजेटी एक्शन जीआईडीएल को दबाने के लिए एक Hole सिंक परत के साथ SOI JLFET प्रस्तुत किया गया है। बरिड ऑक्साइड (BOX) इंजीनियरिंग यानी SOI JLFET के लिए प्रभावी मात्रा में कमी का एहसास करने के लिए उच्च-k BOX को शामिल करना प्रस्तावित है।

Table of Contents

Certificate.....	i
Acknowledgements.....	iii
Abstract.....	v
List of Figures	xv
List of Symbols	xxxiii
Chapter 1: Introduction.....	1
1.1 The Quest for Efficient Switches	1
1.2 The Road Ahead.....	3
1.3 Junctionless FETs.....	6
1.3.1 Working Principle of JLFETs.....	6
1.3.2 Design Constraints for JLFETs	6
1.3.3 Salient Features of JLFETs.....	7
1.3.4 Challenges for JLFETs.....	9
1.3.5 GIDL in JLFETs	10
1.3.6 Motivation Behind the Work Presented on JLFETs	13
1.3.7 Simulation Setup for JLFETs.....	13
1.4 Nanowire FETs	17
1.4.1 Challenges for NWFETs.....	18
1.4.2 GIDL in NWFETs.....	19
1.4.3 Motivation Behind the Work Presented on NWFETs.....	19
1.4.4 Simulation of NWFETs	20
1.5 Thesis Objective.....	23
References.....	24

Chapter 2: Physical Insights into the Nature of Gate Induced Drain Leakage in Ultra-Short Channel Nanowire Field Effect Transistors	30
2.1 Introduction	30
2.2 Device Structure	32
2.3 Results and Discussions	33
2.3.1 Parasitic BJT Action in NW FETs	33
2.3.2 Nature of GIDL in Different NW FET Configurations	35
2.3.3 Impact of Channel Length Scaling	38
2.3.4 Impact of Source Doping	39
2.3.5 Impact of Channel Doping	41
2.3.6 Impact of Drain doping	41
2.3.7 NW FET with a Lightly Doped Souce-Drain Extension	43
2.4 Conclusions	44
References	45
Chapter 3: Diameter Dependency of Leakage Current in Nanowire Junctionless Field Effect Transistors	48
3.1 Introduction	48
3.2 Device Structure	50
3.3 Results and Discussions	50
3.4 Conclusions	56
References	57
Chapter 4: Spacer Design Guidelines for Nanowire FETs from Gate Induced Drain Leakage Perspective	60
4.1 Introduction	60
4.2 Device Structure	61
4.3 Results and Discussions	63
4.3.1 Conventional NWMOSFETs and JAMFETs with Spacer	63

4.3.2	Underlapped NWMOSFETs and JAMFETs with Spacer	65
4.3.3	Impact of Scaling the Gate Length on NWFETs	67
4.3.4	Impact of Spacer on Dynamic Performance of NWFETs	69
4.3.5	Impact of NW Diameter and Underlap Length on L-BTBT	70
4.4	Design Optimization in Sub-10 nm Regime	71
4.5	Conclusions	77
	References	78
Chapter 5: A Novel Gate Stack Engineered Nanowire FET for Scaling to the Sub-10 nm Regime		81
5.1	Introduction	81
5.2	Device Structure	82
5.3	Results and Discussions	82
5.4	Conclusions	90
	References	91
Chapter 6: Comprehensive Analysis of Gate-Induced Drain Leakage in Emerging FET Architectures: Nanotube FETs vs. Nanowire FETs		93
6.1	Introduction	93
6.2	Device Structure	95
6.3	Results and Discussions	96
6.3.1	Impact of Channel Length Scaling	98
6.3.2	Impact of Gate Sidewall Spacer	99
6.3.3	Impact of band gap	100
6.3.4	Drain Bias Sensitivity	102
6.3.5	Impact of Gate Oxide Thickness	102
6.3.6	Impact of core gate diameter	103
6.3.7	Impact of spacer length	104
6.3.8	Impact of doping profile	104

6.4	Conclusions	106
	References.....	107
Chapter 7:_Nanotube Junctionless Field Effect Transistor: Proposal, Design and Investigation.....		111
7.1	Introduction	111
7.2	Device Structure	112
7.3	Results and Discussions	113
7.4	Conclusions	119
	References.....	119
Chapter 8:_Controlling L-BTBT and Volume Depletion in Nanowire JLFETs using Core-Shell Architecture		122
8.1	Introduction	122
8.2	Device Structure	123
8.3	Results and Discussions	124
8.4	Conclusions	129
	References.....	130
Chapter 9:_Insight into Lateral Band-to-Band-Tunneling in Dual-Material Gate Nanowire Junctionless Accumulation Mode Field Effect Transistors		133
9.1	Introduction	133
9.2	Device Structure	134
9.3	Results and Discussions	135
9.4	Conclusions	141
	References.....	142
Chapter 10:_Extended Back Gate JLFET for Scaling to the 5 nm Regime Considering Quantum Confinement Effects		144
10.1	Introduction	144
10.2	Device Structure	145
10.3	Results and Discussions	147

10.4	Conclusions	155
	References.....	156
Chapter 11: Controlling BTBT Induced Parasitic BJT Action in Junctionless FETs using a Hybrid Channel		160
11.1	Introduction	160
11.2	Device Structure	161
11.3	Results and Discussions	163
11.4	Conclusions	166
	References.....	167
Chapter 12: Buried Oxide (BOX) Engineering to Realise Efficient Volume Depletion and Mitigate BTBT Induced Parasitic BJT Action in SOI JLFETs.....		170
12.1	Introduction	170
12.2	SOI JLFET with a high- κ BOX.....	170
12.3	Device Structure	171
12.4	Results and Discussions	172
12.5	Conclusions	179
	References.....	179
Chapter 13: Conclusions		181
13.1	Summary of Contributions	181
13.2	Future Work.....	186
Appendix A.....		188
	Sample Sentaurus Input File for Nanowire JLFETs	188
	Publications based on this work.....	194
	Short Biography	196

List of Figures

Figure 1.1 Impact of scaling the gate length on (a) the switching energy which dictates the dynamic power dissipation and (b) the different power dissipation modes in microprocessors [2]. The evolution of microprocessor (c) power density and (d) clock frequency in last two decades [3].....	2
Figure 1.2 3-D view of a gate-all-around nanowire MOSFET.....	4
Figure 1.3 3-D view of a double gate (DG) n-MOSFET.....	4
Figure 1.4 3-D view of a double gate (DG) n-junctionless FET (JLFET).....	5
Figure 1.5 Different operating regimes of JLFETs: (a) full depletion mode (b) partial depletion mode and (c) flat band mode.....	7
Figure 1.6 Recent publication trend in the field of junctionless FETs (JLFETs). Statistics obtained from web of science using all combinations of keywords (X AND Y), where $X=\{\text{junctionless, JL}\}$ and $Y = \{\text{transistor, FET, MOSFET}\}$	9
Figure 1.7 3-D view of a double gate (DG) junctionless accumulation mode FET (JAMFET).....	10
Figure 1.8 (a) Energy band profiles of the JLFET taken at a cutline 1 nm below the Si-SiO ₂ interface and (b) Hole concentration contour plot of a JLFET in the OFF-state ($V_{GS} = 0.0$ V).	11
Figure 1.9 The figure 5(a) of [26] which clearly indicates that the OFF-state current in ultra-short channel JLFETs is significantly large than the gate leakage current.	12
Figure 1.10 The schematic view of a bulk planar (BP) JLFET.	13
Figure 1.11(a) Simulation models calibrated by reproducing the results of [27]. The tunneling mass of electrons m_e and holes m_h and the effective density of states for holes g_v and electrons g_c are given in the inset (b) Using the calibrated models of (a), the	

quantization models are next calibrated by reproducing the experimental results of [26].	16
Figure 1.12 Recent publication trend in the field of nanowire FETs (NWFETs). Statistics obtained from web of science using all combinations of keywords (X AND Y), where $X=\{\text{nanowire, NW}\}$ and $Y = \{\text{transistor, FET, MOSFET, JLFET, JAMFET}\}$	18
Figure 1.13 (a) Energy band profiles of the NWMOSFET and NWJLFET taken at a cutline 1 nm below the Si-SiO ₂ interface and (b) Experimental transfer characteristics of the vertically stacked (5 storeyed) NW MOSFET and NWJAMFET [18].	20
Figure 1.14 Simulation models calibrated by reproducing the results of [17]. The tunneling mass of electrons m_e and holes m_h and the effective density of states for holes g_v and electrons g_c are given in the inset.	22
Figure 1.15 Using the calibrated models, the validity of the simulation set up is analysed by reproducing the the experimental results of NWJLFETs [23].	23
Figure 2.1 (a) 3-D view and (b) cross sectional view of a nanowire FET.	32
Figure 2.2 The transfer characteristics and (b) the energy-band profiles in the OFF-state at 1 nm below Si-SiO ₂ interface of the different NW FET configurations.	34
Figure 2.3 The hole concentration contour plot at $V_{GS} = 0.0$ V, $V_{DS} = 1.0$ V for (a) NW MOSFET, (b) NW JAMFET and (c) NW JLFET and at $V_{GS} = -1.5$ V, $V_{DS} = 1.0$ V for (d) NW MOSFET, (e) NW JAMFET and (f) NW JLFET.	34
Figure 2.4 Energy-band profiles of (a) NW JAMFET, (b) NW JLFET and (c) NW MOSFET at 1 nm below Si-SiO ₂ interface for different gate voltages.	36
Figure 2.5 Electron current density (J_n) and Hole current density (J_p) contour plot of (a) NW MOSFET, (b) NW JAMFET and (c) NW JLFET for $V_{GS} = -1.5$ V at $V_{DS} = 1.0$ V.	37

Figure 2.6 Impact of gate length scaling on (a) NW JAMFET, (b) NW MOSFET and (c) NW JLFET for $L_g \geq 10$ nm.....	38
Figure 2.7 Impact of gate length (L_g) and nanowire diameter (d_{NW}) scaling to 5 nm with and without the inclusion of the quantum confinement effects on (a) NW JAMFET, (b) NW MOSFET and (c) NW JLFET.	40
Figure 2.8 (a) The transfer characteristics and (b) Energy-band profiles at 1 nm below Si-SiO ₂ interface of the NW JAMFET with different source dopings.	40
Figure 2.9 (a) The transfer characteristics and (b) Energy-band profiles at 1 nm below Si-SiO ₂ interface of the NW MOSFET with different source dopings.....	41
Figure 2.10 (a) The transfer characteristics and (b) Energy-band profiles at 1 nm below Si-SiO ₂ interface of the NW JAMFET with different channel dopings.	41
Figure 2.11 (a) The transfer characteristics and (b) Energy-band profiles at 1 nm below Si-SiO ₂ interface of the NW MOSFET with different channel dopings.....	42
Figure 2.12 (a) The transfer characteristics and (b) Energy-band profiles at 1 nm below Si-SiO ₂ interface of the NW JAMFET with different drain dopings.....	42
Figure 2.13 (a) The transfer characteristics and (b) Energy-band profiles at 1 nm below Si-SiO ₂ interface of the NW MOSFET with different drain dopings.....	42
Figure 2.14 Schematic view of the NW FET with a lightly doped source/drain extension region (LDD) adjacent to the channel region.	43
Figure 2.15 (a) Transfer characteristics and (b) Energy-band profiles at 1 nm below Si-SiO ₂ interface in the OFF-state of conventional NW JAMFET and NW JAMFET with lightly doped extension regions.	43
Figure 2.16 (a) The transfer characteristics and (b) Energy-band profile at 1 nm below Si-SiO ₂ interface in the OFF-state of conventional NW MOSFET and NW MOSFET with lightly doped extension regions.	44
Figure 3.1 3-D view of the nanowire junctionless FET (NWJLFET).	49

Figure 3.2 The transfer characteristics of NWJLFETs with (a) $d_{NW} \leq 10$ nm and (b) $d_{NW} \geq 10$ nm.	50
Figure 3.3 The energy-band profiles of the NWJLFET with (a) $d_{NW} \leq 10$ nm and (b) $d_{NW} \geq 10$ nm at 1 nm below Si-SiO ₂ interface.	52
Figure 3.4 The variation of (a) DIBL without including BTBT model and (b) the source to channel barrier height at 1 nm below Si-SiO ₂ interface in the OFF-state with nanowire diameter.	52
Figure 3.5 The variation of (a) the tunneling width at 1 nm below Si-SiO ₂ interface and (b) the average subthreshold swing of the NWJLFETs with diameter.	53
Figure 3.6 The hole concentration contour plot of the NWJLFET at middle of the channel for various d_{NW} (a) without including BTBT model and (b) with BTBT model in the OFF-state ($V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V).	53
Figure 3.7 The electron concentration contour plot of the NWJLFET at middle of the channel for various d_{NW} (a) without including BTBT model and (b) with BTBT model in the OFF-state ($V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V).	54
Figure 3.8 The variation in (a) the OFF-state current and (b) ON-state current and ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) of the NWJLFET with nanowire diameter.	55
Figure 3.9 (a) The transfer characteristics and (b) the energy-band profiles at 1 nm below the Si-SiO ₂ interface of the NWJLFET with different gate sidewall spacers.	55
Figure 4.1 2-D cross-sectional view of (a) the conventional NWMOSFET and (b) underlapped NWMOSFET with gate sidewall spacers and (c) the conventional NWJAMFET and (d) underlapped NWJAMFET with gate sidewall spacers.	62
Figure 4.2 The transfer characteristics of the conventional (a) n-NWMOSFET and (b) n-NWJAMFET with different gate sidewall spacers.	63
Figure 4.3 The transfer characteristics of the conventional (a) p-NWMOSFET and (b) p-NWJAMFET with different gate sidewall spacers.	64

Figure 4.4 The lateral electric field profile of the (a) conventional n-NWMOSFET with air/HfO ₂ spacer and underlapped n-NWMOSFET with air/HfO ₂ spacer and (b) conventional n-NWJAMFET with air/HfO ₂ spacer and underlapped n-NWJAMFET with air/HfO ₂ spacer.	65
Figure 4.5 Energy band profiles of the conventional (a) n-NWMOSFET and (b) n-NWJAMFET with HfO ₂ and air spacer taken at a cutline 1 nm below the Si-SiO ₂ interface.....	65
Figure 4.6 The transfer characteristics of the (a) conventional n-NWMOSFET with air spacer and the underlapped n-NWMOSFET with different gate sidewall spacers and (b) the conventional n-NWJAMFET with air spacer and the underlapped n-NWJAMFET with different gate sidewall spacers.	66
Figure 4.7 The transfer characteristics of the (a) conventional p-NWMOSFET with air spacer and the underlapped p-NWMOSFET with different gate sidewall spacers and (b) the conventional p-NWJAMFET with air spacer and the underlapped p-NWJAMFET with different gate sidewall spacers.	67
Figure 4.8 Energy band profiles of the (a) conventional NWMOSFET with air spacer and underlapped NWMOSFET with HfO ₂ and air spacer (b) conventional NWJAMFET with air spacer and underlapped NWJAMFET with HfO ₂ and air spacer taken at a cutline 1 nm below the Si-SiO ₂ interface.....	68
Figure 4.9 Impact of scaling the gate length on the conventional (a) NWMOSFET and (b) NWJAMFET with HfO ₂ and air spacer.	68
Figure 4.10 Impact of scaling the gate length on the (a) conventional NWMOSFET with air spacer and underlapped NWMOSFET with HfO ₂ and air spacer and (b) conventional NWJAMFET with air spacer and underlapped NWJAMFET with HfO ₂ and air spacer.	69
Figure 4.11 Gate capacitance (C_{gg}) and intrinsic delay (τ) of the conventional (a) n-NWMOSFET and (b) n-NWJAMFET with different spacers.	70

Figure 4.12 Gate capacitance (C_{gg} and intrinsic delay (τ) of the underlapped (a) n-NWMOSFET and (b) n-NWJAMFET with different spacers.....	71
Figure 4.13 The transfer characteristics of the conventional (a) n-NWMOSFET and (b) n-NWJAMFET with different nanowire diameter.....	71
Figure 4.14 Energy band profiles of the conventional (a) n-NWMOSFET and (b) n-NWJAMFET with air spacer taken at a cutline 1 nm below the Si-SiO ₂ interface for different nanowire diameter (d_{NW}).....	72
Figure 4.15 The transfer characteristics of the (a) n-NWMOSFET and (b) n-NWJAMFET with different underlap lengths (L_U).	72
Figure 4.16 Energy band profiles of the (a) n-NWMOSFET and (b) n-NWJAMFET with air spacer taken at a cutline 1 nm below the Si-SiO ₂ interface for different underlap lengths (L_U).....	72
Figure 4.17 The OFF-state current (I_{OFF}) and the ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) of the conventional (a) n-NWMOSFET and (b) n-NWJAMFET with different spacers.....	73
Figure 4.18 The OFF-state current (I_{OFF}) and the ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) of the underlapped (a) n-NWMOSFET and (b) n-NWJAMFET with different spacers.....	73
Figure 4.19 The output characteristics of the underlapped (a) n-NWMOSFET and (b) n-NWJAMFET with SiO ₂ and air spacer.....	74
Figure 4.20 The OFF-state current (I_{OFF}) and the ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) of the underlapped (a) n-NWMOSFET and (b) n-NWJAMFET with different nanowire diameter (d_{NW}).....	74
Figure 4.21 The OFF-state current (I_{OFF}) and the ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) of the underlapped (a) n-NWMOSFET and (b) n-NWJAMFET with different underlap length (L_U).	75

Figure 4.22 The OFF-state current (I_{OFF}) and the ON-state to OFF-state current ratio ($I_{\text{ON}}/I_{\text{OFF}}$) of the underlapped (a) n-NWMOSFET and (b) n-NWJAMFET with different drain voltage (V_{DS}).....	75
Figure 4.23 Energy band profiles of the conventional (a) n-NWMOSFET and (b) n-NWJAMFET with SiO_2 spacer taken at a cutline 1 nm below the Si-SiO ₂ interface for different drain voltage (V_{DS}).....	76
Figure 4.24 The OFF-state current (I_{OFF}) and the ON-state to OFF-state current ratio ($I_{\text{ON}}/I_{\text{OFF}}$) of the underlapped (a) n-NWMOSFET and (b) n-NWJAMFET with different source/drain extension doping ($N_{\text{S/DEXT}}$).	76
Figure 4.25 Energy band profiles of the conventional (a) n-NWMOSFET and (b) n-NWJAMFET with SiO_2 spacer taken at a cutline 1 nm below the Si-SiO ₂ interface for different source/drain extension doping ($N_{\text{S/DEXT}}$).....	76
Figure 5.1 The cross-sectional view of the (a) DMSG, (b) underlapped ($L_{\text{U}} = 10$ nm) SMG with HfO_2 spacer and (c) conventional ($L_{\text{U}} = 0$ nm) SMG NWMOSFET and (d) DMSG, (e) underlapped ($L_{\text{U}} = 10$ nm) SMG with HfO_2 spacer and (f) conventional ($L_{\text{U}} = 0$ nm) SMG NWJAMFET.	83
Figure 5.2 The transfer characteristics of the conventional SMG, underlapped SMG with HfO_2 spacer and the DMSG (a) NW MOSFET and (b) NW JAMFET with varying ϕ_{M1}	85
Figure 5.3 The electric field profile of the (a) conventional SMG, (b) underlapped SMG with HfO_2 spacer and DMSG with (c) $t_{\text{M2}} = 5$ nm and (d) $t_{\text{M2}} = 3$ nm NWMOSFET in the OFF-state ($V_{\text{GS}} = 0.0$ V, $V_{\text{DS}} = 1.0$ V).	85
Figure 5.4 Energy band profiles of the conventional SMG, underlapped SMG with HfO_2 spacer and the DMSG (a) NW MOSFET and (b) NW JAMFET with varying ϕ_{M1} at a cutline 1 nm below the Si-SiO ₂ interface.....	86
Figure 5.5 Transfer characteristics of the DMSG (a) NW MOSFET and (b) NW JAMFET with different t_{M2}	86

Figure 5.6 Transfer characteristics of the DMSG (a) NW MOSFET and (b) NW JAMFET with different L_s	86
Figure 5.7 Energy band profiles of the DMSG (a) NW MOSFET and (b) NW JAMFET with different L_s at a cutline taken 1 nm below the Si-SiO ₂ interface.	87
Figure 5.8 Transfer characteristics of the DMSG (a) NW MOSFET and (b) NW JAMFET with different types of spacer.....	87
Figure 5.9 Energy band profiles of the DMSG (a) NW MOSFET and (b) NW JAMFET with different spacers at a cutline 1 nm below the Si-SiO ₂ interface.	88
Figure 5.10 Impact of gate length scaling on the conventional SMG and DMSG (a) NW MOSFET and (b) NW JAMFET.....	89
Figure 5.11 Energy band profiles of conventional SMG and DMSG (a) NW MOSFET and (b) NW JAMFET for $L_g = 7$ nm at a cutline 1 nm below the Si-SiO ₂ interface...	89
Figure 5.12 The total gate capacitance (C_{gg}) and the intrinsic delay (τ) of the underlapped SMG with HfO ₂ spacer (filled symbols) and DMSG (open symbols) (a) NW MOSFET and (b) NW JAMFET.....	89
Figure 6.1 3-D view of (a) nanotube (NT) FET and (b) nanowire (NW) FET depicting that NTFETs are essentially NWFETs with a core gate. Cross-sectional view of (c) NTMOSFET and (d) NTJAMFET and (e) NWMOSFET and (f) NWJAMFET. Cutline B-B' has been taken 1 nm below the Si-SiO ₂ interface adjacent to the core gate while cut lines A-A' and C-C' have been taken 1 nm below the Si-SiO ₂ interface adjacent to the outer gate.....	94
Figure 6.2 Transfer characteristics of NT and NWFETs.	96
Figure 6.3 Energy band profiles of (a) NT and NWMOSFET and (b) NT and NWJAMFET. The cut lines A-A', B-B' and C-C' have been taken 1 nm away from the Si-SiO ₂ interface.	97

Figure 6.4 Hole generation rate contour plot of (a) NW and (b) NT JAMFET in the OFF-state ($V_{DS} = 1.0$ V, $V_{GS} = 0.0$ V).....	97
Figure 6.5 Impact of gate length scaling on (a) NT and NW MOSFET and (b) NT and NW JAMFET.....	98
Figure 6.6 Energy band profiles of (a) NT and NWMOSFET and (b) NT and NWJAMFET for $L_g = 7$ nm.	98
Figure 6.7 Variation of (a) OFF-state current (I_{OFF}) and (b) I_{ON}/I_{OFF} of NT and NW FETs with different spacers.	99
Figure 6.8 Energy band profiles taken at a cutline A-A' for NT and C-C' for NW (a) MOSFET and (b) JAMFET with different spacers.....	100
Figure 6.9 Variation of (a) gate capacitance (C_{gg}) and (b) intrinsic delay (τ_D) of the NT and NW FETs with different spacers.....	100
Figure 6.10 Variation of OFF-state current (I_{OFF}) of NT and NW (a) MOSFET and (b) JAMFET with the intrinsic material band gap (E_g).	101
Figure 6.11 Variation of OFF-state current (I_{OFF}) of NT and NW (a) MOSFET and (b) JAMFET with the drain voltage (V_{DS}).	101
Figure 6.12 Variation of ON-state to OFF-state current current ratio (I_{ON}/I_{OFF}) of NT and NW (a) MOSFET and (b) JAMFET with the drain voltage (V_{DS}).	101
Figure 6.13 Variation of OFF-state current (I_{OFF}) of NT and NW (a) MOSFET and (b) JAMFET with the effective gate oxide thickness (EOT).....	102
Figure 6.14 Variation of OFF-state current (I_{OFF}) and I_{ON}/I_{OFF} of NT (a) MOSFET and (b) JAMFET with the core diameter.....	103
Figure 7.1 (a) 3-D view and (b) cross-sectional view at cutline A-A' of the NT JLFET and schematic view of (c) NW JLFET and (d) NW JAMFET.	112

Figure 7.2 (a) Transfer characteristics and (b) energy band profiles taken at a cutline 1 nm below the Si-SiO ₂ interface of the NT JLFET and NW JLFET and NWJAMFET with air and SiO ₂ spacer.....	114
Figure 7.3 (a) Transfer characteristics and (b) energy band profiles taken at a cutline 1 nm below the Si-SiO ₂ interface.....	115
Figure 7.4 Variation of (a) OFF-state current (I_{OFF}) and (b) ON-state to OFF-state current ratio (I_{ON}/I_{OFF}) of the NT and NW JLFETs with different spacers.	116
Figure 7.5 Variation of (a) gate capacitance (C_{gg}) and (b) intrinsic delay (τ) of the NT and NW JLFETs with different spacers.....	117
Figure 7.6 Electric-field contour plot in the OFF-state ($V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V) of NT JLFET for (a) $d_{core} = 10$ nm and (b) $d_{core} = 30$ nm.	117
Figure 7.7 (a) Energy band profiles taken at a cutline 1 nm below the Si-SiO ₂ interface and (b) OFF-state current (I_{OFF}) and I_{ON}/I_{OFF} of the NT JLFETs for different core diameter (d_{core}).	118
Figure 7.8 (a) I_{ON}/I_{OFF} and I_{OFF} and (b) energy band profiles taken at a cutline 1 nm below the Si-SiO ₂ interface of the NT JLFETs ($L_g = 10$ nm) for different spacer lengths.	118
Figure 8.1 Cross-sectional view of the (a) conventional and (b) core-shell (CS) nanowire JLFET (NWJLFET).	123
Figure 8.2 The transfer characteristics and (b) the energy-band profiles in the OFF-state at 1 nm below Si-SiO ₂ interface of the conventional NWJLFET ($d_{nw} = 10$ nm) and the CSJLFET ($d_{nw} = 15$ nm) with different core dopings.....	125
Figure 8.3 The hole concentration contour plot of (a) the conventional NWJLFET ($d_{nw} = 10$ nm) and the CSJLFET ($d_{nw} = 15$ nm, $t_{shell} = 5$ nm) with a core doping of $N_A = 1 \times 10^{19}$ cm ⁻³ at $V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V.	125

Figure 8.4 (a) The transfer characteristics and the energy-band profiles in the OFF-state at (b) a lateral cutline taken 1 nm below Si-SiO ₂ interface and (c) at a vertical cutline taken at the middle of the channel of the conventional NWJLFET ($d_{nw} = 20$ nm) and the CSJLFET ($d_{nw} = 25$ nm).	126
Figure 8.5 The electron concentration contour plot of (a) the conventional NWJLFET ($d_{nw} = 20$ nm) and (b) CSJLFET ($d_{nw} = 25$ nm, $t_{shell} = 10$ nm) with a core doping of $N_A = 1 \times 10^{20} \text{ cm}^{-3}$ at $V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V.....	127
Figure 8.6 The electron concentration contour plot of the cross section of CSJLFET ($d_{nw} = 25$ nm, $t_{shell} = 10$ nm) at the centre of the channel region for a core doping of (a) $N_A = 1 \times 10^{19} \text{ cm}^{-3}$ and (b) $N_A = 1 \times 10^{20} \text{ cm}^{-3}$ at $V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V.....	127
Figure 8.7 The impact of variation in the core doping on I_{ON} and I_{ON}/I_{OFF} of the CSJLFET with (a) $d_{NW} = 15$ nm, $t_{shell} = 5$ nm and (b) $d_{NW} = 25$ nm, $t_{shell} = 10$ nm...	128
Figure 8.8 The impact of variation in the core diameter on I_{ON} and I_{ON}/I_{OFF} of the CSJLFET with (a) $d_{NW} = 15$ nm, $t_{shell} = 5$ nm and (b) $d_{NW} = 25$ nm, $t_{shell} = 10$ nm...	128
Figure 8.9 The impact of scaling on (a) I_{OFF} and (b) I_{ON}/I_{OFF} of the conventional NWJLFET ($d_{nw} = 10$ nm) and the CSJLFET ($d_{nw} = 15$ nm, $t_{shell} = 5$ nm) with a core doping of $N_A = 1 \times 10^{19} \text{ cm}^{-3}$	130
Figure 9.1 (a) 3-D view and (b) the cross-sectional view of the dual-material gate (DMG) NWJLFET.....	134
Figure 9.2 The transfer characteristics of the SMG NWJAMFET and DMG NWJAMFET with $\phi_{con} = 4.5$ eV and varying ϕ_{tun}	135
Figure 9.3 (a) The lateral electric field distribution of the SMG and DMG NWJAMFET and (b) the energy band profiles of the SMG NWJAMFET and DMG NWJAMFET with $\phi_{con} = 4.5$ eV and varying ϕ_{tun} taken at a cutline 1 nm below the Si-SiO ₂ interface.	136

Figure 9.4 (a) The transfer characteristics and (b) the energy band profiles taken at a cutline 1 nm below the Si-SiO ₂ interface of the SMG NWJAMFET and DMG NWJAMFET with $\phi_{\text{tun}} = 3.9$ eV and varying ϕ_{con}	137
Figure 9.5 (a) The transfer characteristics and (b) the energy band profiles taken at a cutline 1 nm below the Si-SiO ₂ interface of the SMG NWJAMFET and DMG NWJAMFET with varying L_c/L_g ratio.....	137
Figure 9.6 (a) The transfer characteristics of the SMG and DMG NWJAMFET with different channel doping and (b) the energy band profiles of the DMG NWJAMFET with varying channel doping at a cutline taken 1 nm below the Si-SiO ₂ interface. ..	137
Figure 9.7 (a) The energy band profiles taken at a cutline 1 nm below the Si-SiO ₂ interface and (b) the transfer characteristics of the DMG NWJAMFET with varying drain doping.	138
Figure 9.8 (a) The transfer characteristics and (b) the energy band profiles taken at a cutline 1 nm below the Si-SiO ₂ interface of the SMG NWJAMFET, SMG NWJLFET, DMG NWJAMFET and DMG NWJLFET ($\phi_{\text{tun}} = 4.2$ eV and $\phi_{\text{con}} = 4.7$ and $L_c/L_g = 0.5$).	139
Figure 9.9 The variation of (a) The transconductance (G_m) and (b) the total gate capacitance (C_{gg}) with the gate voltage for SMG and DMG NWJAMFET.	140
Figure 9.10 (a) The effective drive current (I_{eff}) and the intrinsic delay (τ_D) and (b) the cut-off frequency (f_t) of the SMG and the DMG NWJAMFET.	140
Figure 10.1 Schematic view of (a) the conventional DGJLFET and (b) the extended back gate EBG DGJLFET.	145
Figure 10.2 (a) Transfer characteristics and (b) Energy-band profiles taken at a cutline 1 nm below the top Si-SiO ₂ interface of the conventional DGJAMFET, DGJLFET and the EBG DGJLFET ($L_g = 20$ nm).....	147
Figure 10.3 Hole concentration contour plot of (a) the conventional DGJLFET and (b) the EBG DGJLFET in the OFF-state ($V_{\text{GS}} = 0.0$ V and $V_{\text{DS}} = 1.0$ V).....	148

Figure 10.4 Electron concentration contour plot of (a) the conventional DGJLFET and (b) the EBG DGJLFET in the ON-state ($V_{GS} = 1.0$ V and $V_{DS} = 1.0$ V).....	148
Figure 10.5 (a) The output characteristics of the DGJLFET and the EBG DGJLFET and (b) The schematic view of the EBG DGJLFET with a back gate underlap.....	149
Figure 10.6 (a) The total gate capacitance C_{gg} (at $V_{GS} = 1.0$ V) and (b) the transient response of the CMOS inverter of the conventional DGJLFET and the EBG DGJLFET for different back gate underlap lengths.	150
Figure 10.7 (a) The intrinsic delay and (b) the I_{ON}/I_{OFF} ratio of the DGJLFET and the EBG DGJLFET for different back gate underlap lengths.	150
Figure 10.8 The impact of gate length scaling on the transfer characteristics of the EBG DGJLFET and the DGJLFET for (a) $L_g \geq 10$ nm and (b) $L_g = 5$ nm.....	151
Figure 10.9 Hole concentration contour plot of the conventional DGJLFET in the OFF-state ($V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V) for (a) $L_g = 20$ nm and (b) $L_g = 5$ nm.	151
Figure 10.10 (a) Energy-band profiles at 1 nm below Si-SiO ₂ interface for $L_g = 5$ nm (with $t_{Si} = 5$ nm) and (b) the transfer characteristics for different silicon film thickness (t_{Si}) of the conventional DGJLFET and the EBG DGJLFET.	153
Figure 10.11 (a) The transfer characteristics and (b) the energy band profiles taken at a cutline 1 nm below the Si-SiO ₂ interface of the conventional DGJLFET and the EBG DGJLFET for different doping concentrations.....	154
Figure 10.12 The electron concentration contour plot in the OFF-state ($V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V) of (b) the conventional DGJLFET and (c) the EBG DGJLFET for $N_D = 2 \times 10^{19}$ cm ⁻³	154
Figure 10.13 Transfer characteristics of the conventional DGJLFET and the EBG DGJLFET for different silicon film doping.....	155
Figure 11.1 Schematic view of a p ⁺ hole sink (HS) JLFET.....	162

Figure 11.2 Transfer characteristics of the conventional and the HS JLFET ($L_g = 20$ nm) for different t_{Si} at $V_{DS} = 1.0$ V.	163
Figure 11.3 Energy-band profiles of the conventional SOI JLFET and the HS JLFET at 1 nm below Si-SiO ₂ interface for (a) $V_{GS} = 0.0$ V and (b) $V_{GS} = -0.5$ V at $V_{DS} = 1.0$ V.	164
Figure 11.4 BTBT generation rate contour plot of (a) the conventional SOI JLFET and (b) the HS JLFET in the OFF-state ($V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V).....	164
Figure 11.5 Hole concentration contour plot of (a) the conventional SOI JLFET and (b) the HS JLFET in the OFF-state ($V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V).	165
Figure 11.6 SRH recombination rate contour plot of (a) the conventional SOI JLFET and (b) the HS JLFET in the OFF-state ($V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V).	165
Figure 11.7 The hole current density contour plot of the HS JLFET in the OFF-state ($V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V).....	165
Figure 11.8 The transfer characteristics of (a) the HS JLFET ($t_{Si} = 10$ nm and $t_{HS} = 5$ nm) and (b) the conventional SOI JLFET ($t_{Si} = 5$ nm) for different channel lengths.	166
Figure 12.1 Schematic view of (a) the conventional SOI JLFET and (b) the JLFET with a high- κ BOX (HB JLFET).....	171
Figure 12.2 Suggested process flow to realize the high- κ BOX SOI wafers based on the smart-cut process described in [8].	173
Figure 12.3 Transfer characteristics of the conventional SOI JLFET and the HB JLFET for different BOX thicknesses (t_{BOX}).	174
Figure 12.4 Electron concentration contour plot of (a) the conventional SOI JLFET and (b) the HB JLFET in the thermal equilibrium state ($V_{GS} = 0.0$ V and $V_{DS} = 0.0$ V) and (c) the conventional SOI JLFET and (d) the HB JLFET in the OFF-state ($V_{GS} = 0.0$ V and $V_{DS} = 1.0$ V).	175

Figure 12.5 Variation of (a) the OFF-state leakage current and (b) the ON-state to OFF-state current ratio of the conventional SOI JLFET ($t_{\text{BOX}} = 10 \text{ nm}$) and the HB JLFET ($t_{\text{BOX}} = 10 \text{ nm}$) with the channel length.	175
Figure 12.6 Transfer characteristics of the HB JLFET ($t_{\text{BOX}} = 10 \text{ nm}$) (a) for different ground plane dopings and (b) in the presence of different types of traps.....	176
Figure 12.7 Transfer characteristics of the HB JLFET ($t_{\text{BOX}} = 10 \text{ nm}$) and the conventional SOI JLFET ($t_{\text{BOX}} = 10 \text{ nm}$) with different gate electrode work functions and in the presence of a substrate bias of $-V_{\text{dd}}$	176
Figure 12.8 The variation of $I_{\text{ON}}/I_{\text{OFF}}$ and $I_{\text{ON}}/(I_{\text{OFF}} \times C_g)$ for different substrate bias in the conventional SOI JLFET ($t_{\text{BOX}} = 10 \text{ nm}$).....	177
Figure 12.9 The variation of (a) the gate capacitance (C_g) and (b) the C_{gs} to C_{gd} ratio of the conventional SOI JLFET ($t_{\text{BOX}} = 10 \text{ nm}$) and the HB JLFET ($t_{\text{BOX}} = 10 \text{ nm}$) with the gate voltage.	178
Figure 13.1 The publications in the area of GIDL of emerging nano-devices: NWFETs and JLFETs from different research groups across the world in last 10 years (2007-2017). Statistics obtained from web of science using all combinations of keywords (X AND Y), where $X=\{\text{junctionless, JLFET, nanowire, NWFET, nanowire transistor, junctionless transistor, junctionless MOSFET, nanowire MOSFET, nanowire JLFET, nanowire JAMFET}\}$ and $Y = \{\text{leakage, gate-induced drain leakage, drain leakage, GIDL}\}$	187

List of Tables

TABLE 2.1 Parameters used for the device simulation.....	33
TABLE 3.1 Parameters used for the device simulation.....	49
TABLE 4.1 Parameters used for the device simulation.....	63
TABLE 5.1 Parameters used for the device simulation.....	84
TABLE 6.1 Parameters used for the device simulation.....	95
TABLE 7.1 Parameters used for the device simulation.....	113
TABLE 8.1 Parameters used for the device simulation.....	124
TABLE 10.1 Parameters used for the device simulation.....	146
TABLE 11.1 Parameters used for the device simulation.....	162
TABLE 12.1 Parameters used for the device simulation.....	173
TABLE 12.2 Performance of the HBJLFET in the presence of traps	178

List of Symbols

IC	Integrated Circuits
IoT	Internet of Things
BTBT	Band to Band Tunneling
CMOS	Complementary Metal Oxide Semiconductor
DMG	Dual Material Gate
E_g	Energy band gap of the material
DIBL	Drain Induced Barrier Lowering
DSDT	Direct Source-Drain Tunneling
I_{OFF}	OFF-state Leakage Current
V_{DD}	Supply Voltage
I_{ON}	ON-State current
K	Dielectric constant
L_g	Channel length
P_{stat}	Static Power Dissipation
EOT	Effective Oxide Thickness
BTI	Bias Temperature Instability
GIDL	Gate-induced Drain Leakage
L_U	Underlap Length
L_S	Spacer Length

L_t	Tunnel Gate Length
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SOI	Silicon-on-Insulator
L_m	Misalignment Length
DMG	Dual Material Gate
SMG	Single Material Gate
JLFET	Junctionless Field Effect Transistor
TFET	Tunnel Field Effect Transistor
NWFET	Nanowire Field Effect Transistor
t_{ox}	Gate oxide thickness
t_{si}	Silicon body thickness
JAM	Junctionless Accumulation Mode
d_{NW}	Nanowire Diameter
L_{EXT}	Source/Drain Extension Length
N_{SEXT}	Source Extension Doping
N_{DEXT}	Drain Extension Doping
$N_{Channel}$	Channel Doping
$\Delta\Phi$	Energy range over which tunneling takes place
t_{GP}	Ground plane Thickness
t_{BOX}	BOX Thickness
J_n	Electron Current Density

J_p	Hole Current Density
QC	Quantum Confinement
LDD	Lightly Doped Drain
L_{LDD}	Length of Lightly Doped Drain Extension
DIBT	Drain Induced Barrier Thinning
L-BTBT	Lateral Band-to-Band-Tunneling
T-BTBT	Transverse Band-to-Band-Tunneling
t_{epi}	Source/Drain Epitaxial Length
ϕ_{M1}	Metal 1 Work Function
ϕ_{M2}	Metal 2 Work Function
t_{M1}	Metal 1 Thickness
t_{M2}	Metal 2 Thickness
NT	Nanotube
d_{core}	Core Diameter
t_{gc}	Gate Contact Thickness
t_{shell}	Shell Thickness
Φ_{tun}	Work Function of Tunnel Gate
Φ_{con}	Work Function of Control Gate
C_{gg}	Gate Capacitance
L_p	Pocket Length
C_{gd}	Miller Capacitance (Gate-to-Drain Capacitance)
G_m	Transconductance
f_t	Cut-off Frequency
t_{HS}	Hole Sink Thickness