DESIGN AND ANALYSIS OF EMERGING NANOSCALE JUNCTIONLESS FETS FROM GATE-INDUCED DRAIN LEAKAGE PERSPECTIVE

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by

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Dedicated to

Dada ji, Dadi Maa, Mumma, Papa, Saumya and all the teachers whom I came across at different stages during the last 24 years of my life. Some motivated me, some inspired me, some helped in designing the process flow of my life, often poking me with a sharp stick called "truth", enabling my fabrication in the present form.

कर्मण्येवाधिकारस्ते मा फलेषु कदाचन।
मा कर्मफलहेतुर्भूर्मा ते सङ्गोऽस्त्वकर्मणि॥ २-४७

- *Shrimad Bhagwad Gita, Chapter 2, Verse: 47*

हिन्दी: **कर्म करो फल की चिंता मत करो |**

English: ***You have the right to work only.***

Do not let the expected outcome of your action be your motive, nor

let yourself attach to inaction.

Certificate

This is to certify that the thesis entitled "***Design and Analysis of Emerging Nanoscale Junctionless FETs from Gate-Induced Drain Leakage Perspective"*** being submitted by **Mr. Shubham Sahay** for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under my supervision and guidance. The matter embodied in this thesis has not been submitted for the award of any other degree or diploma.

Date:

Place: New Delhi

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Shubham Sahay

Abstract

CMOS scaling has been the driving machinery behind this era of internet of things (IoT) and big data. However, CMOS scaling has reached its bottleneck owing to the significant power dissipation. The incessant scaling of the MOSFETs has increased the OFF-state leakage current significantly resulting in significantly high static power dissipation. Although scaling the power supply may reduce the static power dissipation, it degrades the ON-state to OFF-state current ratio because of the Botzmann tyranny of 60mV/decade sub-threshold swing in the conventional MOSFETs which arises due to the inherent thermionic conduction mechanism.

Two probable solutions have been proposed to overcome this CMOS scaling bottleneck: (a) alternate device architectures with improved electrostatic gate control like finFETs, gate-all-around nanowire (GAA NW) (b) alternate conduction mechanism i.e. band-to-band-tunneling or impact ionization based steep sub-threshold swing devices such as Tunnel FETs (TFETs) and impact ionization MOS (IMOS).

Although GAA NWFETs offer the best possible gate control leading to suppression of the short channel effects, unfortunately, the efficient gate control results in a considerable band overlap of the valence band of the channel region with the conduction band of the drain region. This facilitates a band-to-band-tunneling (BTBT) of electrons from channel to the drain increasing the OFF-state leakage current significantly. This new component of gate-induced drain leakage (GIDL) known as lateral BTBT (L-BTBT) is unique to the NWFETs and hinders their scaling.

Furthermore, scaling the MOSFETs to the sub-10 nm regime requires ultra-steep doping profiles at the metallurgical junctions. However, realising such an ultra-steep doping profile is extremely difficult. Therefore, FETs without any metallurgical junctions known as junctionless FETs (JLFETs) were proposed. However, the GIDL in JLFETs leads to the formation of a parasitic bipolar junction transistor (BJT) which is triggered in the OFF-state leading to a significantly high leakage current.

Therefore, this thesis addresses this important issue of GIDL in emerging nano-scale FETs which increases the OFF-state leakage current in NWFETs and JLFETs. First, a physical insight into the nature of GIDL in different NWFET configurations is

provided. A parasitic BJT theory is proposed to explain the difference in the nature of NWJLFETs and NWMOSFETs. The diameter dependent dominant leakage mechanisms in the NWJLFETs are then analysed. The spacer design guidelines for: (a) NWFETs without source/drain extension underlap and (b) NWFETs with source/drain extension underlap are provided from a GIDL perspective.

Furthermore, a NWFET with a dual metal stacked gate architecture (DMSG) is proposed to mitigate the GIDL and efficiently scale the NWFETs to the sub-10 nm regime. A comprehensive analysis of GIDL in the recently reported nanotube (NT) FETs which are essentially NWFETs with a core gate is performed. A NTJLFET is also proposed to suppress the GIDL i.e. BTBT induced parasitic BJT action. A core-shell NWJLFET with a p^+-core is proposed to (a) mitigate the BTBT induced parasitic BJT action in NWJLFETs with nanowire diameter < 10 nm and (b) realize efficient volume depletion in NWJLFETs with nanowire diameter >10 nm.

The efficacy of the dual-material gate (DMG) architecture to mitigate the GIDL in NWJAMFETs is also analysed for the first time. An extended back gate architecture for scaling the double gate (DG) JLFETs to the sub-10 nm regime by diminishing the GIDL is proposed. In addition, a SOI JLFET with a hole sink layer to suppress the parasitic BJT action GIDL is presented. Buried oxide (BOX) engineering i.e. inclusion of a high-κ BOX to realize efficient volume depletion is also proposed for SOI JLFETs.

सार

CMOS स्केलिंग (IOT) और बड़े डेटा के इस युग के पीछे ड्राइविंग मशीन रही है। हालांकि, महत्वपूर्ण बिजली अपव्यय के कारण CMOS स्केलिंग अपने bottleneck पर पहुंच गया है। MOSFET के निरंतर स्केलिंग में ऑफ-स्टेट रिसाव की बढ़ोतरी में वृद्धि हुई है जिससे महत्वपूर्ण रूप से उच्च स्थैतिक पावर अपव्यय में वृद्धि हुई है। यद्यपि बिजली की आपूर्ति को स्केलिंग स्थिर शक्ति अपव्यय को कम कर सकती है, यह MOSFET को ON-OFF-स्टेट चालू अनुपात को घटाता है क्योंकि पारंपरिक MOSFET में 60 mV / दशक के sub-threshold स्विंग के बॉटज़मैन tyranny की वजह से थर्मोनिक चालन तंत्र के कारण उत्पन्न होता है। ।

CMOS स्केलिंग बाधाओं से उबरने के लिए दो संभावित समाधान प्रस्तावित किए गए हैं: (ए) बेहतर इलेक्ट्रोस्टैटिक गेट नियंत्रण जैसे FinFETs, गेट-ऑल-नैनोवायर (GAA NW) (बी) वैकल्पिक प्रवाहकत्त्व तंत्र यानी बैंड-टू-बैंड- टनल FET (TFET) और प्रभाव आयनाईकरण MOS (IMOS) जैसे सुरंग या प्रभाव आयनकरण आधारित खड़ी sub-threshold स्विंग डिवाइस।
हालांकि, GAA NWFETs सबसे अच्छा संभव गेट नियंत्रण की पेशकश करते हैं जो कि छोटे चैनल प्रभावों को दमन करने के लिए अग्रणी होता है, दुर्भाग्य से, कुशल गेट नियंत्रण परिणाम, drain क्षेत्र के conduction बैंड के साथ चैनल क्षेत्र के valence बैंड के काफी बैंड ओवरलैप में होता है। यह चैनल से बैंड-टू-बैंड-टनलिंग (BTBT) की सुविधा देता है जिससे ऑफ-स्टेट रिसाव चालू होने से नाले में बढ़ोतरी हो सकती है। पार्श्व बीटीबीटी (L-BTBT) के रूप में जाना गेट से प्रेरित drain रिसाव (GIDL) का यह नया घटक NWFET के लिए अद्वितीय है और अपने स्केलिंग को बाधित करता है। इसके अलावा, MOSFET को उप 10-nm शासन में स्केलिंग करने के लिए धातुकर्म जंक्शनों पर अल्ट्रा-खड़ी डोपिंग प्रोफाइल की आवश्यकता होती है। हालांकि, इस तरह के अल्ट्रा-खड़ी डोपिंग प्रोफाइल का एहसास बेहद मुश्किल है। इसलिए, किसी भी धातुकर्म जंक्शन के बिना FET का प्रस्ताव किया गया था, जिसे Junctionless FET (JLFET) कहा जाता था। हालांकि, JLFET में GIDL एक परजीवी द्विध्रुवी जंक्शन ट्रांजिस्टर (BJT) के गठन की ओर अग्रसर है जो sub-20 nm में शुरू हो रहा है जिससे एक महत्वपूर्ण उच्च रिसाव चालू होता है।

इसलिए, इस थीसिस ने उभरते नैनो पैमाने के FET में GIDL के इस महत्वपूर्ण मुद्दे को संबोधित किया है जो NWFET और JLFET में ऑफ-स्टेट रिसाव को बढ़ाता है। सबसे पहले, विभिन्न NWFET कॉन्फ़िगरेशन में GIDL: की प्रकृति में एक भौतिक अंतर्दृष्टि प्रदान की जाती है। NWJLFETs और NWMOSFETs की प्रकृति में अंतर को स्पष्ट करने के लिए एक परजीवी BJT सिद्धांत प्रस्तावित किया गया है। उसके बाद NWFET में व्यास पर निर्भर प्रभावी sरिसाव तंत्र का विश्लेषण किया जाता है। स्पेसर डिजाइन दिशानिर्देश निम्न के लिए: (ए) Source / drain विस्तार के बिना NWFET और (बी) Source / Drain विस्तार के साथ NWFET GIDL परिप्रेक्ष्य से उपलब्ध कराए जाते हैं।

इसके अलावा, NWFET, एक दोहरी धातु वाली गेट (DMSG) के साथ GIDL को कम करने और उप -10 एनएम शासन के कुशलता से NWFET को स्केल करने का प्रस्ताव है। हाल ही में नैनोट्यूब (NTFET) में GIDL का एक व्यापक विश्लेषण किया गया है जो मुख्य द्वार के साथ अनिवार्य रूप से NWFET हैं। NTJLFET को भी GIDL को दबाने का प्रस्ताव है, अर्थात् BTBT प्रेरित परजीवी बीजेटी कार्रवाई। P -कोर के साथ एक कोर-शंख NWJLFET प्रस्तावित है (ए) NWJLFET में नैनोवायर व्यास के साथ बीटीबीटी प्रेरित परजीवी बीजेटी कार्रवाई को कम कर देता है और (बी) NWJLFETs में nanowire व्यास के साथ> 10 एनएम पर्याप्त मात्रा में कमी महसूस करते हैं।

NWJLFET में GIDL को कम करने के लिए ड्यूल-मेटल gate (DMG) आर्किटेक्चर की प्रभावकारिता का भी पहली बार विश्लेषण किया गया है। GIDL को कम करके उप -10 एनएम शासन के लिए डबल गेट (DG) JLFET स्केलिंग के लिए एक विस्तारित बैक गेट वास्तुकला प्रस्तावित है। इसके अलावा, परजीवी बीजेटी एक्शन जीआईडीएल को दबाने के लिए एक Hole सिंक परत के साथ SOI JLFET प्रस्तुत किया गया है। बरिड ऑक्साइड (BOX) इंजीनियरिंग यानी SOI JLFET के लिए प्रभावी मात्रा में कमी का एहसास करने के लिए उच्च-κ BOX को शामिल करना प्रस्तावित है।

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IC	Integrated Circuits
IoT	Internet of Things
BTBT	Band to Band Tunneling
CMOS	Complementary Metal Oxide Semiconductor
DMG	Dual Material Gate
E_g	Energy band gap of the material
DIBL	Drain Induced Barrier Lowering
DSDT	Direct Source-Drain Tunneling
I_{OFF}	OFF-state Leakage Current
V_{DD}	Supply Voltage
I_{ON}	ON-State current
K	Dielectric constant
L_g	Channel length
P_{stat}	Static Power Dissipation
EOT	Effective Oxide Thickness
BTI	Bias Temperature Instability
GIDL	Gate-induced Drain Leakage
L_U	Underlap Length
L_S	Spacer Length

L_t	Tunnel Gate Length
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
SOI	Silicon-on-Insulator
L_m	Misalignment Length
DMG	Dual Material Gate
SMG	Single Material Gate
JLFET	Junctionless Field Effect Transistor
TFET	Tunnel Field Effect Transistor
NWFET	Nanowire Field Effect Transistor
t_{ox}	Gate oxide thickness
t_{si}	Silicon body thickness
JAM	Junctionless Accumulation Mode
d_{NW}	Nanowire Diameter
L_{EXT}	Source/Drain Extension Length
N_{SEXT}	Source Extension Doping
N_{DEXT}	Rain Extension Doping
$N_{Channel}$	Channel Doping
$\Delta\Phi$	Energy range over which tunneling takes place
t_{GP}	Ground plane Thickness
t_{BOX}	BOX Thickness
J_n	Electron Current Density

J_p	Hole Current Density
QC	Quantum Confinement
LDD	Lightly Doped Drain
L_{LDD}	Length of Lightly Doped Drain Extension
DIBT	Drain Induced Barrier Thinning
L-BTBT	Lateral Band-to-Band-Tunneling
T-BTBT	Transverse Band-to-Band-Tunneling
t_{epi}	Source/Drain Epitaxial Length
ϕ_{M1}	Metal 1 Work Function
ϕ_{M2}	Metal 2 Work Function
t_{M1}	Metal 1 Thickness
t_{M2}	Metal 2 Thickness
NT	Nanotube
d_{core}	Core Diameter
t_{gc}	Gate Contact Thickness
t_{Shell}	Shell Thickness
Φ_{tun}	Work Function of Tunnel Gate
Φ_{con}	Work Function of Control Gate
C_{gg}	Gate Capacitance
L_P	Pocket Length
C_{gd}	Miller Capacitance (Gate-to-Drain Capacitance)
G_m	Transconductance
f_t	Cut-off Frequency
t_{HS}	Hole Sink Thickness