# SIGNAL DELAY STUDIES IN DIGITAL MOS LSI CIRCUITS: AN RC NETWORK APPROACH

*By*

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*THESIS SUBMITTED*
*IN FULFILMENT OF THE REQUIREMENTS FOR*
*THE AWARD OF THE DEGREE OF*
**DOCTOR OF PHILOSOPHY**

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OCTOBER, 1989

# CERTIFICATE

This is to certify that the dissertation,"Signal Delay Studies in Digital MOS LSI Circuits: An RC Network Approach", which is being submitted by Navneet Kumar Jain for the award of degree of Doctor of Philosophy to the Indian Institute of Technology, Delhi is a record of bona fide research work, carried out under our guidance and supervision.

This dissertation has reached the standard of fulfilling the requirements of the regulations relating to the degree. The results obtained in this dissertation have not been submitted to any other University or Institute for the award of any degree or diploma.

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## ACKNOWLEDGEMENTS

I am deeply grateful to my research advisors Prof. A. B. Bhattacharyya and Prof. V. C. Prasad who introduced me into the exciting area of Computer Aided Design Of VLSI and consistently guided with enthusiasm throughout the course of this dissertation.

I wish to express my sincere thanks to Professor S. C. Dutta Roy, Dr. G. S. Visweswaran, Dr. Gopalswamy and Mr. Rajat Gupta for their helpful discussions and comments. I am indebted to Mr. Ashok Sharma for his critical discussions and invaluable suggestions during the course of present work.

My appreciations are due to all of my friends and colleagues for extending their help and good wishes.

Special thanks are also due to the staff of Center for Applied Research in Electronics, I. I. T. Delhi for their excellent technical support. The partial financial support extended by the Department of Electronics, Government of India(National Microelectronics Council) is duly acknowledged.

I would like to thank my brother Anil and sister Karuna for keeping me going and, of course, asking me stimulating questions, such as "when will this ever get done", never failed me to spur me on to greater efforts.

Finally, the patient understanding and cooperation extended throughout the work by my wife Kusum is greatly appreciated. The refreshing interruptions caused by my son Mitava and his cousins Ruchika and Titu made the work pleasant.

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# ABSTRACT

Modelling a digital gate and its fanout interconnections including pass transistors by an RC network is a well accepted practice. These networks may be RC lines/trees/meshes having linear or nonlinear element characteristics. Computation of signal delays, its sensitivity with respect to a design parameter and its voltage waveform properties at any node in an RC network are of interest in timing analysis/simulation. In this thesis some new results on waveform bound, signal delay and delay time sensitivity are presented for a general class of RC networks.

Waveform bound of any node 'e' in an linear nonleaky RC tree/mesh can be obtained using three time constant parameters; $T_{De}$(Elmore's Delay), $T_{Re}$ and $T_p$. A Tree algorithm of order O(n) is used to compute signal dealy $T_{De}$ in an RC tree both for zero and nonzero initial conditions. In general, the computation of signal delays in an RC mesh requires solutions of simultaneous linear equations ($O(n^3)$). In Chapter II, a fast **computational scheme** is developed for computing signal delay in **nonleaky RC mesh**. An RC mesh can be constructed by a series of partial RC networks. Initially, the partial RC network is an RC tree, to which the remaining resistor elements (chords) are added in sequence. Signal delay at the selected nodes of the new partial RC network are updated. The updating scheme is based on updating resistance matrix of a resistor network, to which a resistor element is added between any two nodes. In fact, mutual resistances and time constant parameters of only those nodes are updated where the remaining resistors are to be added along with the nodes of interest. Exploiting the local clustering of the resistor elements in an RC mesh, generalized RC tree concept is applied to reduce the

computational requirement for $T_D$'s. Ordering of the resistor elements in an RC mesh to identify partial RC networks would further reduce the computation time. A scheme based on depth first search is presented. It is shown by a number of examples that updating signal delays using depth first ordering is better than a sparse matrix technique. The formulae for updating of $T_R$'s and $T_P$ are also derived.

**In chapter III,** waveform bounds in a **leaky RC mesh** have been established and these can be easily computed given the resistance matrix of the resistor subnetwork. Using these bounds, signal delay can be estimated. Further a scheme is developed to compute signal delays due to multiple excitations. Signal delays in a nonleaky RC mesh having multiple excitation can be obtained using the superposition property of the voltage response and modelling the RC mesh as leaky RC network. Signal delay computation for **leaky RC tree** has been simplified by developing a **Modified Tree Algorithm.** It is shown that the Modified Tree Algorithm is of linear order, which is same as that of the nonleaky RC tree.

Sensitivity of the output node voltage in a nonleaky RC line is monotonic due to change in any of the conductances. **In Chapter IV,** an adjoint network approach is used to generalize the above result to any node (not just the output node on a linear RC tree and not just an RC line). It is shown that **delay time** $\tau_e$( (time required to achieve a given target voltage) of the voltage response $V_e$ at any node 'e' in a linear RC tree decreases for increase in any of the conductances located on the path between node e and the source. For other conductance it increases for small $\tau_e$ but decreases eventually. The results for monotone sensitivity of grounded conductances and capacitances for a linear RC mesh are also derived using adjoint network approach.

**In Chapter V,** sensitivity of delay time, at any node of a **nonlinear monotone RC**

tree due to change in a nonlinear resistor/capacitor is studied using adjoint network approach. Around t = o, the voltage response rises faster for some nodes and slower for others, if a resistor parameter is varied so as to increase the current through it. This shows that the performance at all nodes cannot be improved at the same time. When the response is close to steady state, the response of all nodes is faster. These results can be used to identify parameters so as to improve the performance at a critical node of the tree. Also these results can be used to find bounds on delay time for small and large target voltages at any node on the RC tree.

**In Chapter VI,** a generalization of **delay time sensitivity** to **leaky RC mesh** for small delay time is presented based on the concept of depth of a node in an RC mesh and its adjoint network. Further it has been shown by exploiting the eigenvalue sensitivity that voltages at all the nodes of a **nonleaky RC mesh** are eventually faster.

# CONTENTS

CHAPTER I INTRODUCTION

CHAPTER II A FAST METHOD FOR COMPUTATION OF SIGNAL DELAYS AND WAVEFORM BOUNDS OF AN RC MESH

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## CHAPTER V DELAY TIME SENSITIVITY IN NONLINEAR MONOTONE RC TREE