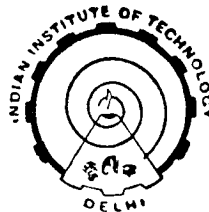


**EFFICIENT SYSTOLIC ARCHITECTURES
FOR
MATRIX, SIGNAL PROCESSING
AND GRAPH RELATED PROBLEMS**

by
M. ZUBAIR

A thesis submitted to the
Indian Institute of Technology, Delhi
for the award of the degree of
DOCTOR OF PHILOSOPHY

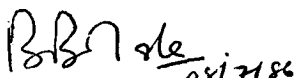


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to my family

CERTIFICATE

This is to certify that the thesis entitled " Efficient Systolic Architectures for Matrix, Signal Processing and Graph Related Problems", being submitted by M.Zubair to the Indian Institute of Technology, Delhi, for the award of the degree of Doctor of Philosophy , is a record of bonafide research work carried out under my supervision. The results contained in this thesis have not been submitted for the award of any degree or diploma.


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Mohd. Zubair
(M. Zubair)

ABSTRACT

In this thesis, we first develop a methodology based on input/output data flow patterns for systolic structures for matrix multiplication. Using this technique it is possible to enforce a desirable input/output data flow pattern. Based on these systolic structures for matrix multiplication, efficient systolic structures for the following matrix related problems have also been obtained:

(i) Adder based systolic structures for (matrix)*(vector) and (matrix)*(matrix) operations: These structures have a considerably higher data throughput rate and ^{are} ~~is~~ independent of the size of the problem and the word length.

(ii) Systolic structures for LU decomposition: We have obtained systolic structures with efficiency 100% and 50%, whereas the previously reported structure for LU decomposition is only 33% efficient [Kun78]. These improved structures are next utilized for solving a system of linear equations.

Similarly, we have obtained efficient systolic structures for the following graph theoretic problems:

(i) A systolic structure for finding bridges in a connected undirected graph: The proposed structure gives improvement in area and time complexity both. It is shown that the proposed systolic structure requires an area $O(n^2)$ and time $O(n)$. In comparison, the one described in [Ull84] takes area $O(n^{2+\epsilon})$, and —

time $O(n^{1+\epsilon})$, for an n -node connected graph. In addition, the new systolic structure requires a simpler control structure.

(ii) A systolic structures for finding strongly connected components in a connected directed graph: This structure has an advantage over the previous structure [Ull84], in terms of having a simpler control structure.

(iii) Systolic structures for computing transitive closure of a connected undirected graph: The newly derived structures avoid the wrap around connections which were present in the previously proposed architecture [Gui79].

A new methodology for synthesizing bit-level systolic array is also developed. This technique is based on SFG representation of the computations. A new SFG rule called the gain transfer is postulated for this purpose. This technique has been successfully applied to obtain systolic structures for IIR filter, discrete convolution and matrix multiplication.

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