ULTRA-WIDE VOLTAGE RANGE SRAMS – CHALLENGES AND DESIGN OF SRAM WITH OPERATING RANGE OF 0.35V-1.20V

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by

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Certificate

This is to certify that the thesis entitled **Ultra-Wide Voltage Range SRAMs – Challenges and Design of SRAM with Operating Range of 0.35V-1.20V** being submitted by **Anuj Grover** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under our supervision and guidance. In our opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any degree or diploma

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To
my parents,
Swaran and Mahender

my wife,
Surya

and our children,
Aarushi and Arunoday

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Anuj Grover

Abstract

An ultra wide voltage range (UWVR) SRAM should achieve high performance and energy-efficiency across a wide range of operational voltages. UWVR SRAMs should achieve these goals without compromising on reliability and error resilience.

In this work we first explore a dual rail SRAM based UWVR solution for SoCs in which SRAM power is not a dominant share of total chip power. We identify the limitations of dual supply SRAMs in enabling aggressive DVFS and propose a Low Standby Power, Capacitively Coupled Sense Amplifier that extends operational voltage range of periphery supply to much lower levels than array supply with high energy-efficiency.

For designs where SRAM power forms a major part of total chip power, we propose a solution by co-designing SRAM cell topology, layout and assist schemes. This approach is well suited for L1 cache design. Operation range of a 32Kb SRAM has been expanded to operate at more than 50MHz at 0.35V to 3GHz at 1.2V across process corners in 28nm UTBB-FDSOI technology.

We propose a Dynamically Strengthened Pull Up (DSPU) 8T cell to improve low voltage write speed, as well as a Differential Read Asymmetric (DRA) 8T cell. These cells are designed to optimize read speed and stability, independent of write related constraints. In this work, we also propose a Data Dependent Dynamic Supply and Body Modulation (D3SBM) write assist scheme that can be easily combined with conventional assist schemes to further lower minimum operational voltage of SRAMs by about 100mV. Along with the cell topology and assist scheme, we also propose a litho-friendly interdigited layout topology that reduces wordline capacitance by more than 50% and enables the use of multiple wordlines and proposed assist schemes to extend high performance operation range of SRAMs.

We also define a figure of merit for low voltage and ultra wide voltage range SRAMs to benchmark benefits of the proposed design techniques in terms of density, energy-efficiency and error resilience. We conclude that the schemes and methods proposed in this work lead to significantly better LV and WVR SRAM implementations and provide additional levers of design optimization to SRAM designers.

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