

**ULTRA-WIDE VOLTAGE RANGE SRAMS –
CHALLENGES AND DESIGN OF SRAM WITH
OPERATING RANGE OF 0.35V-1.20V**

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INDIAN INSTITUTE OF TECHNOLOGY DELHI
DECEMBER 2015**

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ULTRA-WIDE VOLTAGE RANGE SRAMS – CHALLENGES AND DESIGN OF SRAM WITH OPERATING RANGE OF 0.35V-1.2V

by

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Submitted

in fulfilment of the requirements for the degree of Doctor of Philosophy

to the



**Indian Institute of Technology Delhi
December 2015**

Certificate

This is to certify that the thesis entitled **Ultra-Wide Voltage Range SRAMs – Challenges and Design of SRAM with Operating Range of 0.35V-1.20V** being submitted by **Anuj Grover** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under our supervision and guidance. In our opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any degree or diploma

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*To
my parents,
Swaran and Mahender*

*my wife,
Surya*

*and our children,
Aarushi and Arunoday*

Acknowledgements

As I start to write this part of my thesis, numerous memories flood my mind. I am extremely grateful to so many people who have contributed to my life and enabled me to reach this milestone. At the onset I would like to warmly thank my advisor, Prof. G. S. Visweswaran. About 16 years back, he gave me the contact of Mr. Rajamohan Varambally at ST to explore training opportunities (that was during the years when I was pursuing my B.Tech. studies). So, in some sense, I even owe my job to him. He has been very encouraging right from the day when I approached him about six years back to explore possibility of doing research under his guidance. During the research work, he would encourage me to explore in directions I was blinded to and challenge me on my assumptions, prod me to delve deeper and motivate me to keep at it. He has been extremely understanding through all these years, through all the ups and downs that everyone goes through in such long time-frames. I also admire him for the beautiful human being that he is. Over the past years I have learnt immensely from him and I am extremely grateful for having the opportunity to work with him. I would also like to thank my co-advisor Dr. Chittoor Parthasarathy. Partha always ensured that I operated in the ‘real’ world. He would always insist on benchmarking and on translating the technical concepts into ideas that can be readily adopted in designs. He facilitated methods to be able to validate my work and encouraged me to collaborate across teams to be more effective in my research.

I am grateful to Prof. Rakesh Patney, Prof. Preeti Ranjan Panda, and Dr. Shouribrata Chatterjee for agreeing to be a part of my review committee and for their valuable inputs and suggestions through various reviews.

I would like to thank Shamsi Azmi, Promod Kumar, and Rajamohan Varambally, my managers at STMicroelectronics India, for their unrelenting support and guidance. I am grateful to them for being extremely patient and encouraging in the past so many years. I am also thankful to Philippe Magarshack, Indavong Vongsavady, and Jacky Uginet for their encouragement through the project.

This project required me to collaborate with and work alongside colleagues at ST and friends at LETI. I wish to express my heartfelt gratitude to Mohammad Daud, Sidharth Rastogi, Prashant Pandey, Shafquat Jahan Ahmad, Priya Talwar, Firasat Hussain, Lokesh Pandey, Abhishek Jain, Nitin Sharma, Deepak Arora, and Kshitij Verma at ST NOIDA. I am thankful to David Turgis, Jean-Philippe Noel, Fabien Giner, Vincent Huard, Philippe Flatresse, and

Robin Wilson at ST Crolles for all their support in project execution and also for ensuring a healthy working relationship with friends at LETI. I am also thankful to Bastien Giraud, Thomas Benoist, Guillaume Moritz, Ivan-Miro Panadez, Edith Beigne, and Alexandre Velantian at LETI for their contribution in project execution and support for testing the SRAMs at LETI.

I am thankful to my colleagues at ST NOIDA for numerous enriching discussions on a range of topics. I specially thank Amit Chhabra, Shishir Kumar, Tanmoy Roy, Harsh Rawat, Dhori Kedar Janardan, Sidharth Gupta, Dibya Dipti, Piyush Jain, Vivek Asthana, and Radhakrishnan Sithananadam for their support, encouragement and also constructive feedback in different stages of my work. Working with you is a relishing experience, and I look forward to a lot more of it. I am also grateful to my friends and colleagues at IIT Delhi, specially Roohie Kaushik, Avikal Bansal, and Mamta Jain, for their timely support and immense logistical help through different phases of my work.

My friends made my journey delightful over the past so many years. I specially wish to thank Alpana and Amit Bhansali, Priya and Ashu Talwar, Dipali and Muneesh Puri, Lippika and Bhushan Rajani, Shikha and Prashant Pandey, Himangini and Promod, Saima and Shamsi Azmi for all the fun that we have together. I look forward to many more years of camaraderie and friendship. I am also thankful to Sumit, my comrade in the daily ride to office, for bearing with my long rants and sharing your insights.

The last part of this section is reserved for the treasure of my life. My gratitude to these treasures can't be expressed in words. My parents and my wife, Surya, are the pillars without whose kind and continuous support this work would not have been possible. They ensured that I was in the right state of mind to continue this work through the 'highs' and 'lows' that life offered in the entire duration. Their sacrifices can't be enumerated. I can only say that I am grateful to them for being a part of my life and accepting me with all my weaknesses and shortcomings.

And I am extremely grateful to God for bringing me in touch with all these beautiful souls and making them a part of my life. Your hand has worked through me, and through them, all the time. This is an offering to you.

Anuj Grover

Abstract

An ultra wide voltage range (UWVR) SRAM should achieve high performance and energy-efficiency across a wide range of operational voltages. UWVR SRAMs should achieve these goals without compromising on reliability and error resilience.

In this work we first explore a dual rail SRAM based UWVR solution for SoCs in which SRAM power is not a dominant share of total chip power. We identify the limitations of dual supply SRAMs in enabling aggressive DVFS and propose a Low Standby Power, Capacitively Coupled Sense Amplifier that extends operational voltage range of periphery supply to much lower levels than array supply with high energy-efficiency.

For designs where SRAM power forms a major part of total chip power, we propose a solution by co-designing SRAM cell topology, layout and assist schemes. This approach is well suited for L1 cache design. Operation range of a 32Kb SRAM has been expanded to operate at more than 50MHz at 0.35V to 3GHz at 1.2V across process corners in 28nm UTBB-FDSOI technology.

We propose a Dynamically Strengthened Pull Up (DSPU) 8T cell to improve low voltage write speed, as well as a Differential Read Asymmetric (DRA) 8T cell. These cells are designed to optimize read speed and stability, independent of write related constraints. In this work, we also propose a Data Dependent Dynamic Supply and Body Modulation (D3SBM) write assist scheme that can be easily combined with conventional assist schemes to further lower minimum operational voltage of SRAMs by about 100mV. Along with the cell topology and assist scheme, we also propose a litho-friendly interdigitated layout topology that reduces wordline capacitance by more than 50% and enables the use of multiple wordlines and proposed assist schemes to extend high performance operation range of SRAMs.

We also define a figure of merit for low voltage and ultra wide voltage range SRAMs to benchmark benefits of the proposed design techniques in terms of density, energy-efficiency and error resilience. We conclude that the schemes and methods proposed in this work lead to significantly better LV and WVR SRAM implementations and provide additional levers of design optimization to SRAM designers.

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