

TOPOLOGICAL EVOLUTION, DESIGN AND ANALYSIS OF QUASI Z-SOURCE EQUIVALENT DC-DC CONVERTERS

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**TOPOLOGICAL EVOLUTION, DESIGN AND ANALYSIS OF
QUASI Z-SOURCE EQUIVALENT DC-DC CONVERTERS**

by

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CERTIFICATE

This is to certify that the thesis entitled “**TOPOLOGICAL EVOLUTION, DESIGN AND ANALYSIS OF QUASI Z-SOURCE EQUIVALENT DC-DC CONVERTERS**” being submitted by Mr. Punit Kumar for the award of degree of Doctor of Philosophy is a record of a bonafide research work carried out by him in the Department of Electrical Engineering of Indian Institute of Technology Delhi, New Delhi.

Mr. Punit Kumar worked under my guidance and supervision and has fulfilled the requirement for the submission of the thesis, which to my knowledge has reached the requisite standards. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any Degree or Diploma.

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ABSTRACT

The work presented in this thesis mainly addresses the design and analysis of new dc-dc boost converter topologies which provide higher voltage gain at lower duty ratio. The traditional Z-source and quasi-Z-source dc-dc converter topologies exhibit voltage gain of $1/(1-2D)$ which is low. In an attempt to increase the voltage gain, firstly two new high gain topologies are evolved in this thesis. The basis for these evolutions is the quasi-Z-source dc-dc converter. The first topology is switched-inductor switched-capacitor based quasi-Z-source dc-dc converter (SLSCQZSC) which is evolved by replacing the inductors of the quasi-Z-source dc-dc converter with switched-inductor cells. While the second topology formulated is L-C-L cell based Z-source dc-dc converter (LCLZSC) which is obtained after replacing the inductor of the traditional Z-source dc-dc converter with an L-C-L cell. Both these topologies exhibit high voltage gain due to the term $1/(1-3D)$. Detailed steady-state and small-signal analysis is established for both these topologies and illustrative simulation and experimental results are presented to validate the topological features.

The above introduced two topologies (i.e. SLSCQZSC and LCLZSC) though exhibit high voltage gain but use more number of components. Additionally, the source current is discontinuous in nature. To alleviate the problem of discontinuous input current and to also minimize the number of components, two more topologies are formulated on the basis of quasi-Z-source dc-dc converter with embedded switched-capacitor cell. These are quasi-Z-network plus switched-capacitor dc-dc boost converter (ZSCBC) and L-C-L cell based quasi-Z-network dc-dc boost converter (LCLQZSC). The maximum voltage gain achieved with these topologies is $(3-3D)/(1-3D)$. Detailed steady-state and small-signal analysis is established. Parameter selection for simulations and prototype development, the design expressions are formulated for inductors and capacitors. To validate the analytical findings, experimental results are presented. Exhaustive investigation revealed that these topologies are

better than the traditional Z-source dc-dc converter topologies as they exhibit low stress on the devices in addition to having the feature of common ground between the source and load.

The ZSCBC and LCLQZSC topologies draw pulsating input current and thus exhibit higher source current ripple. With the motivation to reduce this source current ripple and yet to realize high voltage gain, four quasi-Z-source equivalent dc-dc converters are evolved. The basis for all these topologies is the fourth-order quasi-z-source equivalent dc-dc boost converter (FOEBC) which essentially ensures low source current ripple. To enhance the voltage gain, a switched-capacitor cell is integrated on the up-stream side. Detailed steady-state and small-signal analysis is established and sample experimental results are presented. The comparison of proposed converters is also presented to highlight their merits and demerits. Detailed investigation revealed that these quasi-Z-source equivalent dc-dc converter topologies exhibit the following features: (i) low voltage stress on the devices to improve the reliability, (ii) fewer number of components to increase the efficiency and (iii) continuous input current to reduce source current ripple leading to lower electro-magnetic interference problems.

सारांश

इस थीसिस में प्रस्तुत कार्य मुख्य रूप से नए डीसी-डीसी बूस्ट कन्वर्टर टोपोलॉजी के डिजाइन और विश्लेषण को संबोधित करते हैं जो कम शुल्क अनुपात पर उच्च वोल्टेज लाभ प्रदान करते हैं। पारंपरिक जेड-स्रोत और अर्ध-जेड-स्रोत डीसी-डीसी कनवर्टर टोपोलॉजी $1/(1-2)$ डी के वोल्टेज लाभ को प्रदर्शित करते हैं जो कम है। वोल्टेज लाभ को बढ़ाने के प्रयास में, इस थीसिस में सबसे पहले दो नए उच्च लाभ टोपोलॉजी विकसित किए गए हैं। इन विकासों का आधार अर्ध-जेड-स्रोत डीसी-डीसी कनवर्टर है। पहला टोपोलॉजी स्विच-इंडक्टर स्विच-कैपेसिटर आधारित कैसी-जेड-सोर्स डीसी-डीसी कन्वर्टर (एसएलएससीक्यूजेडएससी) है जो स्विच-इंडक्टर सेल के साथ अर्ध-जेड-सोर्स डीसी-डीसी कनवर्टर के इंडक्टर्स को बदलकर विकसित किया गया है। जबकि दूसरी टोपोलॉजी तैयार की गई एल-सी-एल सेल आधारित जेड-सोर्स डीसी-डीसी कनवर्टर (एलसीएलजेडएससी) है जो पारंपरिक जेड-सोर्स डीसी-डीसी कनवर्टर के इंडक्टर को एल-सी-एल सेल के साथ बदलने के बाद प्राप्त की जाती है। ये दोनों टोपोलॉजी $1/(1-3D)$ शब्द के कारण उच्च वोल्टेज लाभ प्रदर्शित करते हैं। इन दोनों टोपोलॉजी के लिए विस्तृत स्थिर-अवस्था और लघु-संकेत विश्लेषण स्थापित किया गया है और टोपोलॉजिकल विशेषताओं को मान्य करने के लिए उदाहरण सिमुलेशन और प्रयोगात्मक परिणाम प्रस्तुत किए गए हैं।

ऊपर दिए गए दो टोपोलॉजी (यानी एसएलएससीक्यूजेडएससी और एलसीएलजेडएससी) पेश किए गए हैं, हालांकि उच्च वोल्टेज लाभ प्रदर्शित करते हैं लेकिन अधिक संख्या में घटकों का उपयोग करते हैं। इसके अतिरिक्त, स्रोत धारा प्रकृति में असंतत है। असंतत इनपुट करंट की समस्या को कम करने के लिए और घटकों की संख्या को कम करने के लिए, एम्बेडेड स्विच-कैपेसिटर सेल के साथ अर्ध-जेड-स्रोत डीसी-डीसी कनवर्टर के आधार पर दो और टोपोलॉजी तैयार की जाती हैं। ये अर्ध-जेड-नेटवर्क प्लस स्विच-कैपेसिटर डीसी-डीसी बूस्ट कन्वर्टर (जेडएससीबीसी) और एल-सी-एल सेल आधारित अर्ध-जेड-नेटवर्क डीसी-डीसी बूस्ट कन्वर्टर (एलसीएलक्यूजेडएससी) हैं। इन टोपोलॉजी के साथ प्राप्त अधिकतम वोल्टेज लाभ $(3-3D)/(1-3D)$ है। विस्तृत स्थिर-अवस्था और लघु-संकेत विश्लेषण स्थापित

किया गया है। सिमुलेशन और प्रोटोटाइप विकास के लिए पैरामीटर चयन, इंडक्टर्स और कैपेसिटर के लिए डिज़ाइन अभिव्यक्ति तैयार की जाती है। विश्लेषणात्मक निष्कर्षों को मान्य करने के लिए, प्रयोगात्मक परिणाम प्रस्तुत किए जाते हैं। व्यापक जांच से पता चला है कि ये टोपोलॉजी पारंपरिक जेड-सोर्स डीसी-डीसी कनवर्टर टोपोलॉजी से बेहतर हैं क्योंकि वे स्रोत और लोड के बीच सामान्य जमीन की सुविधा के अलावा उपकरणों पर कम तनाव प्रदर्शित करते हैं।

जेडएससीबीसी और एलसीएलक्यूजेडएससी टोपोलॉजी स्पंदनशील इनपुट करंट खींचते हैं और इस प्रकार उच्च स्रोत करंट रिपल प्रदर्शित करते हैं। इस स्रोत के वर्तमान तरंग को कम करने और अभी तक उच्च वोल्टेज लाभ का एहसास करने की प्रेरणा के साथ, चार अर्ध-जेड-स्रोत समकक्ष डीसी-डीसी कन्वर्टर्स विकसित किए गए हैं। इन सभी टोपोलॉजी का आधार चौथे क्रम का अर्ध-जेड-स्रोत समकक्ष डीसी-डीसी बूस्ट कनवर्टर (एफओईबीसी) है जो अनिवार्य रूप से कम स्रोत वर्तमान तरंग सुनिश्चित करता है। वोल्टेज लाभ को बढ़ाने के लिए, एक स्विच-कैपेसिटर सेल को अप-स्ट्रीम साइड पर एकीकृत किया जाता है। विस्तृत स्थिर-अवस्था और लघु-संकेत विश्लेषण स्थापित किया गया है और नमूना प्रयोगात्मक परिणाम प्रस्तुत किए गए हैं। प्रस्तावित कन्वर्टर्स की तुलना उनकी खूबियों और कमियों को उजागर करने के लिए भी प्रस्तुत की जाती है। विस्तृत जांच से पता चला कि ये अर्ध-जेड-स्रोत समकक्ष डीसी-डीसी कनवर्टर टोपोलॉजी निम्नलिखित विशेषताएं प्रदर्शित करते हैं: (i) विश्वसनीयता में सुधार के लिए उपकरणों पर कम वोल्टेज तनाव, (ii) दक्षता बढ़ाने के लिए घटकों की कम संख्या और (iii) सोर्स करंट रिपल को कम करने के लिए निरंतर इनपुट करंट जिससे इलेक्ट्रो-मैग्नेटिक इंटरफेरेंस की समस्या कम होती है।

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LIST OF ABBREVIATIONS

PV	Photovoltaic
BDC	Basic Boost DC-DC Converter
ZSI	Z-source Inverter
QZSI	Quasi-Z-source Inverter
QZN	Quasi-Z-network
SL	Switched-inductor
ZSC	Z-source DC-DC Converter
CCM	Continuous Conduction Mode
QZSC	Quasi-Z-source DC-DC Converter
DCM	Discontinuous Conduction Mode
SC	Switched-capacitor
SLSCQZSC	Switched-inductor Switched-capacitor based Quasi-Z-source DC-DC Converter
LCLZSC	Z-network plus L-C-L cell based DC-DC Converter
ZSCBC	Quasi-Z-network plus Switched-capacitor DC-DC Boost Converter
LCLQZSC	L-C-L cell based Quasi-Z-network DC-DC Boost Converter
FOEBC	Fourth-order Quasi-Z-source Equivalent DC-DC Boost Converter
SCZEBC	Switched-capacitor Quasi-Z-source Equivalent DC-DC Boost Converter
LCLQEBC	L-C-L cell based Quasi-Z-source Equivalent DC-DC Boost Converter
KVL	Kirchoff's Voltage Law
D	Duty Ratio

M	Voltage Gain
KCL	Kirchoff's Current Law
ESR	Equivalent series resistance
CD	Capacitor and Diode
SOQZSC	Sixth order Quasi-Z-source DC-DC Converter
$G_c(s)$	Controller transfer function
RHP	Right Half of s-plane
GM	Gain Margin
PM	Phase Margin
LSCRFBC	Low Source Current Ripple Fourth-order Boost Converter
CP	Charge Pump
S	Sensitivity
T	Complimentary Sensitivity
M_s	Maximum Sensitivity
PWM	Pulse Width Modulation
RMS	Root Mean Square
r_{DS}	on-state resistance
R_F	Diode forward resistance
V_F	Diode forward voltage drop

LIST OF SYMBOLS

V_C	Average Voltage across capacitor
V_g	Source Voltage
V_0	Load Voltage
I_L	Average Current Through Inductor
I_g	Source Current
I_0	Load Current
i_L	Instantaneous Current Through Inductor
Δi_L	Current Ripple Through Inductor
i_C	Instantaneous Current Through Capacitor
v_C	Instantaneous Voltage Across Capacitor
Δv_C	Voltage Ripple Across Capacitor
v_D	Instantaneous Voltage Across Diode
v_S	Instantaneous Voltage Across Switch
V_D	Peak Voltage Across Diode
V_S	Peak Voltage Across Switch
I_D	Average Current Through Diode
I_S	Average Current Through Switch
r	Inductor dc resistance
r_C	Capacitor equivalent series resistance
X_{ss}	Steady-state Solution

$G_{vd}(s)$	Control-to-output transfer function
η	Efficiency
P_0	Load Power