# SUPPRESSING LATERAL BAND-TO-BAND TUNNELING IN JUNCTIONLESS AND ACCUMULATION MODE SOI FETs, NANOWIRE FETs AND NANOTUBE FETs

**AAKASH KUMAR JAIN**

**DEPARTMENT OF ELECTRICAL ENGINEERING**

**INDIAN INSTITUTE OF TECHNOLOGY DELHI**

**JUNE 2020**

**©Indian Institute of Technology Delhi (IITD), New Delhi, 2020**

# SUPPRESSING LATERAL BAND-TO-BAND TUNNELING IN JUNCTIONLESS AND ACCUMULATION MODE SOI FETs, NANOWIRE FETs AND NANOTUBE FETs

by

**AAKASH KUMAR JAIN**

**Department of Electrical Engineering**

*Submitted*

***in fulfillment of the requirements of degree of Doctor of Philosophy***

*to the*

**INDIAN INSTITUTE OF TECHNOLOGY DELHI**

**JUNE 2020**

*Dedicated to*

*My family and all the teachers whom I came across at*

*different stages during my life.*

# CERTIFICATE

This is to certify that the thesis entitled "**Suppressing Lateral Band-To-Band Tunneling In Junctionless And Accumulation Mode SOI FETs, Nanowire FETs And Nanotube FETs**" being submitted by **Mr. Aakash Kumar Jain** for the award of the degree of Doctor of Philosophy in the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under my supervision and guidance. The matter embodied in this thesis has not been submitted for the award of any other degree or diploma.

Date: $26^{th}$ June, 2020

Place: New Delhi

Dr. Mamidala Jagadesh Kumar

Professor

Department of Electrical Engineering

Indian Institute of Technology Delhi

Hauz Khas, New Delhi-110016, India

# Acknowledgments

---

It is hard to say where to begin when writing a few words of thanks such as these while compiling the thesis. Earning a doctorate in any field of study is years long process that starts long before one enters a graduate school.

First and foremost, I would like to express my profound respect, deepest admiration and sincere thanks to my thesis supervisor Prof. M. Jagadesh Kumar who kept his faith in me and always enhanced my research abilities throughout the course of learning from him. His patience, breadth of knowledge, persistence, and insistence on proper scientific rigour have been a lifelong example for me**.** Furthermore, it was the course on microelectronics offered by him that played a key role in understanding and solving the problems that are presented in this thesis. His teachings on leading a simple and disciplined life have truly been a source of inspiration for me.

I would like to express my sincere acknowledgment to Prof. Madhusudan Singh for introducing me to the field of material synthesis and device fabrication. I got the opportunity to learn about actual cleanroom practices and would like to thank him for providing his valuable and sage advice which are helpful in the management of an experimental project in many matters. I would also like to thank my present and past research committee members Prof. Mukul Sarkar, Prof. Abhisek Dixit, Prof. Sameer Sapra, Prof. Manan Suri, and Prof. Rajendra Singh for their periodic reviews and inputs.

I would also like to acknowledge Nanoscale Research Facility (NRF) and Central Research Facility (CRF) for providing me an opportunity of hands-on experience on various fabrication and

characterization tools in a short period of time. I would also like to acknowledge the past and present colleagues of our research group for their continuous support and guidance. In particular, Dr. Shubham Sahay, Dr. Avikal Bansal, Dr. Avinash Lahgere, and Mr. Jaspreet Singh for their informative technical discussions and motivation during the final stages of this work. I am highly grateful to high performance computational (HPC) facility at IIT Delhi for providing me the resources to carry out the extensively robust simulations at a faster pace leading to a timely finish of this thesis. Last but not the least, I would like to thank my family members who have shaped me into the person that I have been fortunate to become.

# Abstract

The aggressive scaling of silicon CMOS technology has been the key driving catalyst in nearly all technological achievements in today's revolutionary era of supercomputing. However, CMOS scaling is nearly hitting its saturation regime owing to the significant power dissipation arising due to the detrimental short channel effects. The constant field scaling driven by the supply voltage scaling and device miniaturization has accommodated the power dissipation for few decades but is, however, limited by the Boltzmann tyranny of 60 mV/decade which imposes a stringent constraint to the lower limit of the supply voltage scaling. Therefore, it is imperative to push our focus towards alternate emerging device topologies and engineer them for establishing a new foundation for unconventional non-planar devices to continue the incessant scaling trend.

Therefore, in this regard, SOI FETs and multi-gate FET architectures of gate-all-around nanowires (NW) and core-shell nanotube (NT) have gained fair attention to mitigate the concerns of the short channel effects. However, at advanced technology nodes, the need for accomplishing the sharp junctions with a very steep gradient profile is indispensable for realizing the ultra-short channel FETs which requires complex fabrication and costly annealing techniques. In recent years, junctionless (JL) FETs and junctionless accumulation mode (JAM) FETs have proved to be very instrumental in overcoming these stringent requirements of ultra-steep metallurgical junctions and exhibits a lower susceptibility to the short channel effects.

The amalgamation of JLFETs and JAMFETs on the emerging platforms of SOI, NW and NT architectures are expected to offer the optimum performance and enhanced immunity over the short channel effects. Unfortunately, SOI- JLFET exhibits a unique leakage mechanism of inefficient

volume depletion which considerably rises their OFF-state leakage current. Furthermore, addressing the leakage mechanism results in a substantial band overlap of the valence band of the channel region with the conduction band of the drain region leading to an additional leakage component namely lateral band-to band-tunneling (L-BTBT). Thus, the simultaneous suppression of both the leakage mechanism in JLFETs is itself a challenge. Moreover, the L-BTBT is quite amplified in the architectures with the efficient electrostatic gate control and is, therefore, considered as gate induced drain leakage (GIDL) which is unique to NW and NT topologies. The L-BTBT not only rises the OFF-state current which increases the static power dissipation but also results in a degraded sub-threshold swing, and a suppressed source-channel barrier height which facilitates drain–induced barrier lowering and parasitic BJT action in OFF-state and negative gate bias regime. All these issues are against the device scaling and therefore, compensates the promising benefits of SOI, NW and NT configurations for adoption in future technology nodes.

Therefore, this doctoral thesis investigates the feasible ways to address the aforementioned leakage issues in JLFETs and JAMFETs on the variety of emerging platforms to facilitate their scaling to the ultra-short channel regime without adopting any sub-60 mV/dec steep subthreshold mechanisms. First, the leakage mechanism of inefficient volume depletion and detrimental L-BTBT in SOI-JLFETs is simultaneously addressed by the incorporation of a ground plane at shallow depth in the high-k Buried oxide (BOX). The proposed configuration can realize the efficient volume depletion, and, therefore, relaxes the constraints of an ultra-thin silicon body for SOI-JLFET and circumvents the need for complex device architectures for achieving the same. Furthermore, the device presents sustainable immunity to the process variations of doping and film thickness along with the reduced short channel effects.

The NW JAMFETs exhibits a pronounced L-BTBT induced parasitic BJT action in the OFF-state as well in the negative gate bias regime. Therefore, the role of doping profiles in emerging NW

JAMFETs is studied from the perspective of L-BTBT. Various doping profiles are investigated in the channel and drain regions to explore the individual effect of region-wise doping profile on the L-BTBT. Next, the efficacy of gate-on-drain overlap is also analyzed to diminish the dominant L-BTBT induced GIDL in NW JAMFETs without degrading their enhanced ON-state current.

The detrimental lateral band-to-band tunneling (L-BTBT) governing the OFF-state performance of the junctionless (JL) FETs is more pronounced in recently demonstrated nanotube (NT) transistor architectures. Therefore, for the first time, the application of a dual-material gate (DMG) is explored in the emerging NT junctionless accumulation mode FETs to alleviate the enhanced detrimental L-BTBT. The incorporation of DMG reduces the OFF-state current in the NT JAMFETs by more than two orders of magnitude leading to a substantial ON-state to OFF-state current ratio. The essential design guidelines for DMG NT JAMFETs are also provided in terms of the work function of the dual gates and their respective lengths. It is also shown that the DMG NT JAMFET exhibits a reduced gain in $I_{ON}/I_{OFF}$ at the scaled gate lengths owing to the increased sensitivity of the NT JAMFETs to the gate length modulation and a reduced effective gate length.

Furthermore, a symmetric intrinsic pocketed NT JLFET and NT JAMFET architecture is proposed which has narrow intrinsic pockets on both sides of the channel region leading to a diminished L-BTBT induced lateral parasitic BJT action. We demonstrate that the inclusion of the intrinsic pockets greatly alleviates the L-BTBT originated parasitic BJT action and facilitates the scaling of NT architecture to a gate length of 10 nm. Additionally, the proposed architectures exhibit lower sensitivity to the gate length modulation, unlike their conventional counterpart. The proposed architecture exhibits superior immunity against the short channel effects of threshold-voltage roll-off due to the reduced electrostatic source/channel-to-drain coupling. Furthermore, incorporating gate engineering of the dual-material gate (DMG) with the proper tuning of the dual metal gate work functions further enhances the performance of the proposed architectures.

# सार

आज के क्रांतिकारी युग में लगभग सभी तकनीकी उपलब्धियों में सिलिकॉन CMOS तकनीक की आक्रामक स्केलिंग प्रमुख ड्राइविंग उत्प्रेरक रही है। हालांकि, CMOS स्केलिंग लगभग अपने संतृप्ति शासन के कारण हानिकारक लघु चैनल प्रभावों के कारण उत्पन्न होने वाली महत्वपूर्ण बिजली अपव्यय के कारण है। आपूर्ति वोल्टेज स्केलिंग और उपकरण लघुकरण द्वारा संचालित निरंतर क्षेत्र स्केलिंग ने कुछ दशकों के लिए बिजली अपव्यय को समायोजित किया है, लेकिन, 60 mV/dec के बोल्ट्जमैन नियम द्वारा सीमित है, जो आपूर्ति वोल्टेज स्केलिंग की निचली सीमा के लिए एक कठोर बाधा डालता है। । इसलिए, वैकल्पिक उभरती हुई डिवाइस टोपोलॉजी की ओर हमारा ध्यान केंद्रित करना आवश्यक है और निरंतर स्केलिंग प्रवृत्ति को जारी रखने के लिए गैर-पारंपरिक गैर-प्लानर उपकरणों के लिए एक नई नींव स्थापित करने के लिए उन्हें अभियांत्रिकी करना आवश्यक है।

इसलिए, इस संबंध में, SOI FETs और गेट-ऑल-अराउंड नैनोवायर (NW) और कोर-शेल नैनोट्यूब (NT) के मल्टी-गेट FET आर्किटेक्चर ने लघु चैनल प्रभावों की चिंताओं को कम करने के लिए उचित ध्यान दिया है। हालांकि, उन्नत प्रौद्योगिकी नोड्स में, एक बहुत ही खड़ी ढाल प्रोफ़ाइल के साथ तेज जंक्शनों को पूरा करने की आवश्यकता अति लघु चैनल FET को साकार करने के लिए अपरिहार्य है जिसमें जटिल निर्माण और महंगी तकनीकों की आवश्यकता होती है। हाल के वर्षों में, जंक्शन रहित (JL) FETs और जंक्शन रहित संचय मोड (JAM) FETs अल्ट्रा-स्टेप मेटलर्जिकल जंक्शनों की इन कठोर आवश्यकताओं को पार करने में बहुत महत्वपूर्ण साबित हुए हैं और लघु चैनल प्रभावों के लिए कम संवेदनशीलता दिखाते हैं।

SOI, NW और NT आर्किटेक्चर के उभरते प्लेटफार्मों पर JLFETs और JAMFETs के समामेलन से लघु चैनल प्रभावों पर इष्टतम प्रदर्शन और बढ़ी हुई प्रतिरक्षा की पेशकश करने की उम्मीद है। दुर्भाग्य से, SOI-

JLFET ने अकुशल मात्रा में कमी का एक अनूठा रिसाव तंत्र प्रदर्शित किया है, जो उनके ऑफ-स्टेट रिसाव वर्तमान को काफी बढ़ाता है। इसके अलावा, अपवाहनीय मात्रा में कमी के रिसाव तंत्र को संबोधित करते हुए, चैनल क्षेत्र के वैलेंस बैंड के एक पर्याप्त बैंड ओवरलैप के परिणामस्वरूप नाली क्षेत्र के प्रवाहकत्त्व बैंड के साथ एक अतिरिक्त रिसाव घटक अर्थात् पार्श्व बैंड-टू-बैंड-टनलिंग (L-BTBT) होता है। इस प्रकार, JLFETs में दोनों रिसाव तंत्र का एक साथ दमन अपने आप में एक चुनौती है। इसके अलावा, एल-बीटीबीटी आर्किटेक्चर में कुशल इलेक्ट्रोस्टैटिक गेट नियंत्रण के साथ काफी प्रवर्धित है और इसलिए, गेट प्रेरित नाली रिसाव (GIDL) के रूप में माना जाता है जो एनडब्ल्यू और एनटी टोपोलॉजी के लिए अद्वितीय है। L-BTBT न केवल ऑफ-स्टेट करेंट को बढ़ाता है, जो स्टैटिक पॉवर डिसऑर्डर को बढ़ाता है, बल्कि एक डिग्रेडेड सब-थ्रेशोल्ड स्विंग में भी परिणत होता है, और एक दबा हुआ स्रोत-चैनल बैरियर ऊंचाई, जो कि ऑफ-डेड-बैरियर लोअरिंग और पैरासिट BJT एक्शन को बंद करता है। -स्टेट और नकारात्मक गेट पूर्वाग्रह शासन। ये सभी मुद्दे डिवाइस स्केलिंग के खिलाफ हैं और इसलिए, भविष्य की प्रौद्योगिकी नोड्स में गोद लेने के लिए SOI, NW और NT कॉन्फ़िगरेशन के होनहार लाभों की भरपाई करते हैं।

अतः, यह डॉक्टरेट थीसिस JLFET और JAMFET में उपरोक्त रिसाव के मुद्दों को हल करने के लिए संभव तरीकों की जांच करता है, जो कि किसी भी उप-60 mV/dec सब-थ्रेशोल्ड स्विंग मैकेनिज्म को बिना अपनाए अल्ट्रा-शॉर्ट चैनल शासन को स्केल करने के लिए उभरते प्लेटफार्मों की विविधता पर आधारित है। सबसे पहले, SOI-JLFET में अकुशल मात्रा में कमी और हानिकारक L-BTBT के रिसाव तंत्र को एक साथ उच्च-एप्सिलॉन ऑक्साइड (बीओएक्स) में उथले गहराई पर एक ग्राउंड प्लेन के निगमन द्वारा संबोधित किया जाता है। प्रस्तावित विन्यास कुशल मात्रा में कमी को महसूस करने में सक्षम है, और इसलिए, SOI-JLFET के लिए अल्ट्रा-पतली सिलिकॉन बॉडी की बाधाओं को शांत करता है और उसी को प्राप्त करने के लिए जटिल डिवाइस आर्किटेक्चर की आवश्यकता को दरकिनार करता है। इसके अलावा, डिवाइस कम लघु चैनल प्रभावों के साथ डोपिंग और फिल्म की मोटाई की विविधताओं को संसाधित करने के लिए स्थायी प्रतिरक्षा प्रस्तुत करता है।

NW JAMFETs ऑफ-स्टेट के साथ-साथ नकारात्मक गेट पूर्वाग्रह शासन में एक स्पष्ट L-BTBT प्रेरित परजीवी BJT कार्रवाई प्रदर्शित करता है। इसलिए, हम L-BTBT के परिप्रेक्ष्य से उभरते NW JAMFETs में डोपिंग प्रोफाइल की भूमिका की जांच करते हैं। L-BTBT पर क्षेत्र-वार डोपिंग प्रोफाइल के व्यक्तिगत प्रभाव का पता लगाने के लिए चैनल और नाली क्षेत्रों में विभिन्न डोपिंग प्रोफाइल की जांच की जाती है। इसके बाद, NW JAMFET में प्रमुख L-BTBT प्रेरित GIDL को कम करने के लिए गेट-ऑन-ड्रेन ओवरलैप की प्रभावकारिता का विश्लेषण किया जाता है, उनके उन्नत ऑन-स्टेट करंट को घटाए बिना।

JLFET के ऑफ-स्टेट प्रदर्शन को नियंत्रित करने वाले हानिकारक पार्श्व बैंड-टू-बैंड टनलिंग (L-BTBT) हाल ही में प्रदर्शित नैनोट्यूब (NT) ट्रांजिस्टर आर्किटेक्चर में अधिक स्पष्ट है। इसलिए, पहली बार, एक दोहरी सामग्री गेट (DMG) के अनुप्रयोग को उभरते हुए NT JLFET में पता लगाया गया है ताकि बढ़ी हुई हानिकारक L-BTBT को समाप्त किया जा सके। DMG को शामिल करने से NT JAMFETs में ऑफ-स्टेट करंट कम हो जाता है, जो परिमाण के दो आदेशों से अधिक ऑफ-स्टेट वर्तमान अनुपात में होता है। हम दोहरी फाटकों और उनके संबंधित लंबाई के कार्य समारोह के संदर्भ में NTFETs के लिए आवश्यक डिजाइन दिशानिर्देश भी प्रदान करते हैं। हम यह भी दिखाते हैं कि DMG NT JAMFET, $I_{ON}$ / $I_{OFF}$ में स्केल गेट की लंबाई कम करने के लिए NT JAMFETs की बढ़ती संवेदनशीलता के कारण गेट लंबाई मॉडुलन और एक कम प्रभावी गेट लंबाई के कारण कम प्रदर्शित करता है।

इसके अलावा, एक सममित आंतरिक NT JLFET और NT JAMFET में आंतरिक जेब के अनुप्रयोग का प्रस्ताव है जो, जिसमें चैनल क्षेत्र के दोनों किनारों पर संकीर्ण आंतरिक जेब होती है, जो L-BTBT प्रेरित पार्श्व परजीवी टीटी कार्रवाई को कम करने के लिए प्रस्तावित है। आंतरिक जेब को शामिल करने से L-BTBT परजीवी बीजेटी कार्रवाई उत्पन्न होती है और 10 nm की गेट लंबाई तक NT आर्किटेक्चर की स्केलिंग की सुविधा मिलती है। इसके अतिरिक्त, प्रस्तावित आर्किटेक्चर अपने पारंपरिक समकक्ष के विपरीत, गेट लंबाई मॉडुलन के लिए कम संवेदनशीलता प्रदर्शित करते हैं। प्रस्तावित आर्किटेक्चर कम इलेक्ट्रोस्टैटिक स्रोत / चैनल-टू-ड्रेन युग्मन के

कारण थ्रेशोल्ड-वोल्टेज रोल-ऑफ के लघु चैनल प्रभावों के खिलाफ बेहतर प्रतिरक्षा प्रदर्शित करता है। इसके अलावा, दोहरी धातु गेट कार्य कार्यों की उचित ट्यूनिंग के साथ दोहरी सामग्री गेट (DMG) के गेट इंजीनियरिंग को शामिल करना प्रस्तावित आर्किटेक्चर के प्रदर्शन को और बढ़ाता है।

# Table of Contents

List of Figures ........ xv

List of Tables ........ xxiii

List of Acronyms ........ xxv

List of Symbols ........ xxvii

Chapter 1 ........ 1

1.1 Scaling trends in Conventional MOSFETs ........ 1

1.2 The Road ahead: New technology Platforms ........ 6

1.2.1 Full Depleted (FD) SOI MOSFETs ........ 8

1.2.2 Multi-gate MOSFET ........ 9

1.2.2.1 Gate all around Nanowire MOSFET ........ 10

1.2.2.2 Nanotube MOSFET ........ 12

1.3 Junctionless FETs: A promising configuration ........ 17

1.3.1 Working Principle of JLFETs ........ 19

1.3.2 Design Constraints for JLFETs ........ 19

1.3.3 Salient Features of JLFETs ........ 21

1.4 Junctionless Accumulation Mode FETs ........ 23

1.5 Lateral band-to-band tunneling induced GIDL and Parasitic BJT action ........ 24

1.6 Motivation Behind the Work ........ 28

1.7 Simulation Set-up and Model Calibration ........ 28

1.8 Research Objectives and Outline of the Dissertation ........ 33

References .......... 35

Chapter 2 .......... 49

Sub-10 nm Scalability of Junctionless FETs using a Ground Plane in High-κ BOX .......... 49

2.1 Introduction .......... 49

2.2 Device Architecture .......... 51

2.3 Results and Discussions .......... 53

2.4 Scalability in Sub-10 nm regime .......... 61

2.5 Conclusions .......... 65

References .......... 65

Chapter 3 .......... 69

Investigating the Doping Profiles in Nanowire Junctionless Accumulation Mode FETs from the L-BTBT perspective .......... 69

3.1 Introduction .......... 69

3.2 Device Structure .......... 70

3.3 Results and Discussion .......... 73

3.3.1 Channel Profile Optimization .......... 73

3.3.2 Drain Profile Optimization .......... 74

3.3.2.1 Gaussian Doped Drain Extension Profile .......... 75

3.3.2.2 Box Doped Drain Extension Profile .......... 75

3.4 Conclusion .......... 78

References .......... 78

Chapter 4 .......... 81

Controlling L-BTBT in the Nanowire Junctionless Accumulation FETs using Overlapping Gate-On-Drain............ 81
4.1 Introduction ........ 81
4.2 Device Structure ........ 82
4.3 Results and Discussion ........ 84
4.3.1 NW JAMFET with Gate-On-Drain Overlap ........ 84
4.3.2 Device Performance at scaled gate lengths ........ 87
4.4 Conclusions ........ 90
References ........ 91
Chapter 5 ........ 93
Controlling L-BTBT in Emerging Nanotube Accumulation Mode FETs Using Dual-Material Gate ........ 93
5.1 Introduction ........ 93
5.2 Device Structure ........ 94
5.3 Results and Discussions ........ 98
5.3.1 Role of the Control gate ($L_{Con}$) ........ 99
5.3.2 Role of the Auxiliary gate ($L_{aux}$) ........ 100
5.3.3 Role of the gate length ratios ($L_{con}$/ $L_g$) ........ 103
5.3.4 Design optimization in the sub-20 nm regime ........ 105
5.3.4.1 Analysis of DMG NT JAMFET for the gate length of 15 nm ........ 105
5.3.4.2 Analysis of DMG NT JAMFET for the gate length of 10 nm ........ 107
5.4 Conclusions ........ 110
References ........ 111

Chapter 6 ........ 115

Investigation of the Scalability of Emerging Nanotube Junctionless and Accumulation Mode FETs using an Intrinsic Pocket ........ 115

6.1 Introduction ........ 115

6.2 Device Architecture ........ 117

6.3 Results and Discussions ........ 119

6.3.1 Operation of a $P_i$- NT JLFET ........ 120

6.3.2 Performance of $P_i$ -NT JLFETs at scaled gate lengths ........ 130

6.3.3 Performance Analysis of NT JAMFET and $P_i$- NT JAMFET ........ 132

6.3.3.1 Parasitic BJT action in $P_i$-NT JAMFETs ........ 132

6.3.3.2 Scalability of $P_i$ -NT JAMFETs ........ 136

6.3.4 Gate Engineered $P_i$- NT Transistors ........ 139

6.4 Conclusions ........ 144

References ........ 145

Chapter 7 ........ 147

Conclusions and Future Perspectives ........ 147

7.1 Summary of Contributions ........ 147

7.2 Future Perspectives ........ 154

Appendix A ........ 157

Sample Input Deck for simulating a Nanotube JLFET in TCAD Sentaurus ........ 157

List of Publications ........ 165

Biography ........ 167

# List of Figures

Fig. 1.1. Evolution of the various leading processor manufacturers showing the increase in transistor count with the progress of time in accordance with Moore's law [4]............................ 2

Fig. 1.2.(a) Current vs. Voltage plot of an ideal switch. (b) Rise in the OFF-state current ($I_{OFF}$) with the lowering of the threshold voltage. ..................................................................... 3

Fig. 1.3.(a) Clock frequency over the last few decades depicts that the clock frequency has nearly plateaued [3]. (b) Evolution of power consumption density over the last two decades shows a gradual rise [3]. ................................................................................................................ 5

Fig. 1.4. Scaling trend of dynamic and static power dissipation in microprocessors [11]. ............ 6

Fig. 1.5. 3-D schematic view of a conventional bulk planar MOSFET........................................ 7

Fig. 1.6. 3-D schematic view of a UTB FDSOI MOSFET........................................................... 8

Fig. 1.7. 3-D schematic view of (a) Double-gate (DG) MOSFET, and (b) Extended back gate (EBG) DG MOSFET. .................................................................................................... 9

Fig. 1.8. 3-D schematic view of a tri-gate FinFET device............................................................ 9

Fig. 1.9. 3-D schematic view of a gate-all-around nanowire MOSFET ...................................... 11

Fig. 1.10. 3-D schematic view of a Nanotube MOSFET with core-shell gate stacks. ................. 13

Fig. 1.11. Top view of a NT FET with core-shell gate stacks. ................................................... 13

Fig. 1.12. A cross-sectional view of a vertical NT FET with high-κ metal gate stack and spacer regions................................................................................................................................ 16

Fig. 1.13. 3-D schematic view of a DG JLFET. ........................................................................ 18

Fig. 1.14. Various operating regimes of JLFETs: (a) full depletion mode (b) partial depletion mode and (c) flat band mode .............................................................................................. 20

Fig 1.15. 3-D schematic view of a DG JAMFET. ........................................................................ 24

Fig. 1.16. Energy Band diagram of Nanowire JLFET in OFF-state.............................................. 26

Fig. 1.17. Transfer characteristics of (a) NW JFET and NT JLFET, and (b) NW JAMFET and NT JAMFET for a gate length of 20 nm.............................................................................................. 26

Fig. 1.18.(a) Transfer characteristics of NW JLFET and NW JAMFET, and (b) OFF-state energy band profiles of NW JLFET and NW JAMFET.......................................................................... 27

Fig 1.19. Hole generation rate in (a) NT JLFET, and (b) NT JAMFET in the OFF-state............ 27

Fig. 1.20.(a) Simulation models calibrated by reproducing the experimental results of a long channel JLFET reported in [49]. (b) Using the calibrated models of (a), the BTBT model is next calibrated by reproducing the results of [57]. .................................................................... 31

Fig. 1.21. Simulation set-up calibrated by reproducing the reported experimental results of NW MOSFET [92]. ................................................................................................................. 31

Fig. 1.22. Using the calibrated models, the validity of the simulation set up is analyzed by reproducing the experimental results of NW JLFETs [78]......................................................... 32

Fig. 2.1. Schematic view of the GP- JLFET with a high-κ BOX……………………………..51

Fig. 2.2. Suggested fabrication process flow based on the smart-cut process to realize the high-κ BOX SOI substrate with a ground plane........................................................................... 53

Fig. 2.3.(a) Transfer characteristics of (a) SOI-JLFET with $SiO_2$ BOX (b) GP-JLFET with high-κ $HfO_2$ BOX.................................................................................................................... 54

Fig. 2.4.(a) Transfer characteristics of GP- JLFET with high-κ BOX (b) Energy band profiles in the OFF-state for a gate length of 20 nm. .......................................................................... 55

Fig. 2.5. Electric field profile of the SOI JLFET and GP JLFET in the OFF-state ($V_{DS}$ = 1.0 V and $V_{GS}$ = 0.0 V) for a gate length of 20 nm. ........................................................................... 55

Fig. 2.6.(a) Hole concentration contour plot for (a) SOI-JLFET with $SiO_2$ BOX (b) GP-JLFET with $HfO_2$ BOX in the OFF-state ($V_{GS}$ = 0.0 V and $V_{DS}$ = 1.0 V). ............................................ 57

Fig. 2.7. Hole concentration contour plot for (a) SOI-JLFET with $SiO_2$ BOX (b) GP-JLFET with $HfO_2$ BOX at $V_{GS}$ = - 0.5 V and $V_{DS}$ = 1.0 V. ................................................................ 58

Fig. 2.8. Transfer characteristics of the GP-JLFET for 20 % increase in (a) silicon film thickness and (b) silicon film doping. ........................................................................................ 59

Fig. 2.9. The electrostatic potential contour of GP JLFET and SOI JLFET for the $d_{GP}$ of 10 nm and 5 nm in the OFF-state ($V_{GS}$ =0 V and $V_{DS}$ = 1.0 V). .................................................... 60

Fig. 2.10. DIBL and $V_{th}$-roll-off of GP-JLFET at the scaled gate lengths. ................................. 60

Fig. 2.11.(a) Transfer characteristics of GP- JLFET with high-κ BOX at scaled gate lengths (b) Energy band profiles in the OFF-state taken at a cutline 1 nm below the Si/$SiO_2$ interface. for various scaled gate lengths. ........................................................................................ 62

Fig. 2.12. Transfer characteristics of GP-JLFET and SOI- JLFET for a gate length of 7 nm for different drain biases. ........................................................................................ 63

Fig. 2.13. Drain-bias sensitivity of OFF-state current in GP-JLFET and SOI-JLFET. ............... 63

Fig. 2.14 $I_{ON}/I_{OFF}$ of GP-JLFET as a function of drain bias. .................................................... 64

Fig. 3.1. 3-D Schematic view and cross-sectional view of a conventional NW JAMFET.........71

Fig. 3.2. The cross-sectional view of a NW JAMFET with a box doping profile in the channel with the uniformly doped drain. ........................................................................................ 72

Fig. 3.3. The cross-sectional view of a NW JAMFET with a gaussian doping profile in both the channel as well as in the drain region. ........................................................................ 72

Fig. 3.4. The cross-sectional view of a NW JAMFET with a gaussian doping profile in the channel and box doping profile in the drain region. ........................................................................ 72

Fig. 3.5.(a) Transfer characteristics of NW JAMFET for various channel doping profiles with uniform drain-extension doping. (b) OFF-state energy band profiles of NW JAMFET for various channel doping profiles taken at a cutline 1 nm below the Si/$SiO_2$ interface. .............................. 74

Fig. 3.6. (a) Transfer characteristics of NW JAMFET for Gaussian doping profiles in drain with various channel doping profiles. (b) OFF-state energy band profiles of NW JAMFET for various gaussian drain doping profiles at a cutline 1 nm below the Si/$SiO_2$ interface. ............................ 76

Fig. 3.7. (a) Transfer characteristics of NW JAMFET for various box-doped drains doping profiles with a Gaussian channel doping, and (b) OFF-state energy band profiles of NW JAMFET for various drain doping profiles taken at a cutline 1 nm below the Si/$SiO_2$ interface. ..................... 77

Fig. 4.1. (a) 3-D schematic view and (b) Cross-sectional view of a NW JAMFET with gate-on-drain overlap……………………………………………………………………………..83

Fig. 4.2. Transfer characteristics of a conventional NW JAMFET for various gate lengths........ 85

Fig. 4.3. (a) Transfer characteristics of overlapping gate-on-drain NW JAMFETs for various gate overlap lengths with a channel length of 20 nm. (b) Energy band profiles in OFF-state taken at a cutline 1 nm below Si/$SiO_2$ interface for the overlapping gate-on-drain NW JAMFETs with various gate overlap lengths. ........................................................................................................ 86

Fig. 4.4. L-BTBT induced hole generation rate in the channel region of (a) Conventional JAMFET, and (b) Overlapping gate-on-drain JAMFET for a channel length of 20 nm. .............................. 86

Fig. 4.5. (a) Transfer characteristics of overlapping gate-on-drain NW JAMFETs for various gate overlap lengths with a channel length of 10 nm, and (b) Energy band profiles in OFF-state taken at a cutline 1 nm below Si/$SiO_2$ interface for the overlapping gate-on-drain NW JAMFETs with various gate overlap lengths......................................................................................................... 88

Fig. 4.6.(a) Transfer characteristics of overlapping gate-on-drain NW JAMFETs for various gate overlap lengths with a channel length of 7 nm, and (b) Energy band profiles in OFF-state taken at a cutline 1 nm below $Si/SiO_2$ interface for the overlapping gate-on-drain NW JAMFETs with various gate overlap lengths. 88

Fig. 4.7. Comparison of the OFF-state current of NW JAMFETs for the silicon thickness of 10 nm and 5 nm for various overlap lengths ($L_{OV}$). 89

Fig. 5.1. (a) 3-D schematic of the DMG NT JAMFET. (b) Cross-sectional view of DMG NT JAMFET. Cutline A-A' is taken at 1 nm below the $Si/SiO_2$ interface proximate to the core gate. 95

Fig. 5.2. Transfer characteristics of the SMG NT JAMFET for various gate lengths. 98

Fig. 5.3 (a) Transfer characteristics of DMG NT JAMFET, and (b) OFF-state Energy band profiles of a DMG NT JAMFET taken at a cutline A-A' for varying $\Phi_{con}$ at a fixed $\Phi_{aux}$ of 4.2 eV. 99

Fig. 5.4 (a) Transfer characteristics, and (b) OFF-state energy band profiles of DMG NT JAMFET for varying $\Phi_{aux}$ at a fixed $\Phi_{con}$ of 5.2 eV. 101

Fig. 5.5. Lateral electric field of SMG NT JAMFET and DMG NT JAMFET taken at a cutline A-A' at a fixed $\Phi_{aux}$ of 4.2 eV. 102

Fig. 5.6 (a) Transfer characteristics of DMG NT JAMFET and (b) OFF-state energy band profiles of DMG NT JAMFET with varying $L_{con}/L_g$ ratio at $\Phi_{aux}$ = 4.2 eV and $\Phi_{con}$ = 5.2 eV. 104

Fig. 5.7. Transfer characteristics of DMG NT JAMFET by (a) varying $\Phi_{aux}$ at a fixed $\Phi_{con}$ = 5.2 eV and (b) varying $\Phi_{con}$ at a fixed $\Phi_{aux}$ = 4.2 eV. 106

Fig. 5.8. Transfer characteristics of DMG NT JAMFET by varying $L_{con}/L_g$ ratio at $\Phi_{aux}$ = 4.2 eV and $\Phi_{con}$ = 5.2 eV for $L_g$ = 15 nm. 107

Fig. 5.9. Transfer characteristics of DMG NT JAMFETs for (a) varying $\Phi_{aux}$ at a fixed $\Phi_{con}$ = 5.2 eV, and (b) for varying $\Phi_{con}$ at a fixed $\Phi_{aux}$ = 4.5 eV. ............................................................ 108

Fig. 5.10. Transfer characteristics of DMG NT JAMFETs for various $L_{con}/L_g$ ratio after fixing $\Phi_{aux}$ = 4.5 eV and $\Phi_{con}$ = 5.5 eV for $L_g$ = 10 nm. ............................................................ 109

Fig. 5.11. Variation of OFF-state current ($I_{OFF}$) of a DMG NT JAMFET with the spacer length ($L_S$). ............................................................ 110

Fig. 6.1. 3-D schematic of (a) Conventional NT transistor, and (b) Proposed $P_i$-NT transistor. Cross-sectional view of (c) Conventional NT transistor, and (d) Proposed $P_i$- NT transistor. Cutline A-A' is taken at 1 nm below the Si/$SiO_2$ interface. ............................................................ 118

Fig. 6.2. Transfer characteristics of a conventional NT JLFET and NT JAMFET for various gate lengths. ............................................................ 120

Fig. 6.3. (a) Energy band profiles and (b) Electric field profiles of conventional NT JLFET and proposed $P_i$-NT JLFET in the OFF-state for a gate length of 20nm. Profiles are taken at a cutline A-A' 1nm below the Si/$SiO_2$ interface. ............................................................ 121

Fig. 6.4. Hole concentration contour plot for (a) NT JLFET (b) $P_i$- NT JLFET ($L_P$ = 10 nm) in the OFF-state. ............................................................ 122

Fig. 6.5. Electron concentration contour plot for (a) NT JLFET (b) $P_i$- NT JLFET ($L_P$ = 10 nm) in the OFF-state. ............................................................ 122

Fig. 6.6 (a) Transfer characteristics, and (b) OFF-state energy band profiles of a $P_i$-NT JLFET taken at a cutline A-A' 1 nm below the Si/$SiO_2$ interface for various pocket lengths. .............. 124

Fig. 6.7 (a) ON-state current loss and $I_{ON}/I_{OFF}$ ratio of a $P_i$-NT JLFET due to variation in pocket length, and (b) Impact of individual pocket on the ON-state current loss of $P_i$- NT JLFET ($L_P$ =10 nm). ............................................................ 125

Fig. 6.8 Threshold voltage of $P_i$- NT JLFET for various pocket lengths. The pocket length of 0 nm corresponds to conventional NT JLFET. ........................................................................ 126

Fig. 6.9 (a) Transfer characteristics and (b) OFF-state Energy band profiles of a NT JLFET with a pocket on the source side, drain side and both sides ($P_i$-NT transistors). ................................. 127

Fig. 6.10 (a) ON-state energy band profiles of NT JLFET and $P_i$-NT JLFET. (b) Drain-bias sensitivity of OFF-state current in NT JLFET and $P_i$-NT JLFET. ........................................... 129

Fig. 6.11 (a) Transfer characteristics of NT JLFET and $P_i$-NT JLFET (b) OFF-state Energy band profiles of NT JLFET and $P_i$-NT JLFET taken at a cutline A-A'. ........................................... 131

Fig. 6.12 $V_{th}$ roll-off of NT JLFET and $P_i$- NT JLFET at scaled gate lengths. ......................... 132

Fig. 6.13 (a) Electric field and (b) Energy band of NT JAMFET and Pi-NT JAMFET in the OFF-state at a cutline A-A' 1nm below the Si/$SiO_2$ interface. ........................................................ 133

Fig. 6.14 (a) Transfer characteristics, and (b) OFF-state energy band profiles of a $P_i$-NT JAMFET for various pocket lengths taken at the cutline A-A' 1nm below the Si/$SiO_2$ interface. ........... 134

Fig. 6.15 Threshold voltage of $P_i$- NT JAMFET for various pocket lengths. The pocket length of 0 nm corresponds to a conventional NT JAMFET. ................................................................ 136

Fig. 6.16 (a) ON-state current loss and $I_{ON}/I_{OFF}$ ratio of a $P_i$-NT JLFET due to variation in pocket length, and (b) Impact of individual pocket on the ON-state current loss of $P_i$- NT JLFET ($L_P$ =10 nm). ......................................................................................................................... 136

Fig.6.17.(a) Transfer characteristics, and (b) OFF-state energy band profiles of NT JAMFET and $P_i$-NT JAMFET taken at a cutline A-A' 1nm below the Si/$SiO_2$ interface. .............................. 137

Fig. 6.18.(a) Drain-bias sensitivity of OFF-state current in $P_i$-NT JAMFET and (b) Threshold voltage roll-off of $P_i$-NT JAMFET. ........................................................................................ 138

Fig. 6.19. Cross-sectional view of a dual-material gate (DMG) $P_i$- NT transistor. ................... 139

Fig. 6.20. Transfer characteristics of (a) NT JLFET, $P_i$-NT JLFET, and DMG-$P_i$-NT JLFET, and (b) NT JAMFET, $P_i$-NT JAMFET and DMG-$P_i$- NT JAMFET. .............................................. 140

Fig. 6.21. OFF-state energy band profiles of (a) NT JLFET, $P_i$-NT JLFET and DMG-$P_i$- NT . 141

Fig. 6.22. Transfer characteristics of $P_i$-NT JAMFET and DMG $P_i$-NT JAMFET for $L_g$ = 10 nm. ........................................................................................................................... 142

Fig. 6.23 Subthreshold swing of (a) NT JLFET, $P_i$- NT JLFET and $P_i$- NT JLFET .................. 143

# List of Tables

Table 2.1 .......... 54

Table 2.2 .......... 64

Table 3.1 .......... 71

Table 4.1 .......... 83

Table 4.2 .......... 89

Table 5.1 .......... 97

Table 6.1 .......... 119

Table 7.1 .......... 119

# List of Acronyms

| | |
|---|---|
| BJT | Bipolar Junction Transistor |
| BPJLT | Bulk planar Junctionless Transistor |
| BTBT | Band-to-Band Tunneling |
| BOX | Buried oxide |
| CMOS | Complementary Metal Oxide Semiconductor |
| DIBL | Drain Induced Barrier Lowering |
| DG | Double Gate |
| DIBT | Drain Induced Barrier Thinning |
| DMG | Dual Material Gate |
| EOT | Effective Oxide Thickness |
| FD | Fully Depleted |
| GIDL | Gate Induced Drain Leakage |
| GAA | Gate all around |
| GP | Ground Plane |
| IC | Integrated Circuit |
| IoT | Internet of Things |
| JL | Junctionless |
| JAM | Junctionless Accumulation Mode |

| | |
|---|---|
| JLFET | Junctionless Field Effect Transistor |
| JAMFET | Junctionless Accumulation Mode Field Effect Transistor |
| L-BTBT | Lateral Band-to-Band Tunneling |
| MOSFET | Metal Oxide Semiconductor Field Effect Transistor |
| NW | Nanowire |
| NT | Nanotube |
| NW JLFET | Nanowire Junctionless Field Effect Transistor |
| NW JAMFET | Nanowire Junctionless Accumulation Mode Field Effect Transistor |
| NT JLFET | Nanotube Junctionless Field Effect Transistor |
| NT JAMFET | Nanotube Junctionless Accumulation Mode Field Effect Transistor |
| SCE | Short Channel Effects |
| SS | Subthreshold Swing |
| SMG | Single Material Gate |
| SOI | Silicon on Insulator |
| T-BTBT | Transverse Band-to-Band-Tunneling |
| UTB | Ultra-thin Body |
| WKB | Wentzel-Kramers-Brillouin |

# List of Symbols

| | |
|---|---|
| $I_{OFF}$ | OFF-state Current |
| $I_{ON}$ | ON-State current |
| $I_{ON}/I_{OFF}$ | ON-state to OFF-state current ratio |
| $E_g$ | Energy band gap of the material |
| $L_g$ | Gate length |
| $L_{eff}$ | Effective Channel Length |
| $L_s$ | Spacer Length |
| $\kappa$ | Dielectric constant |
| $P_s$ | Static Power Dissipation |
| $t_{ox}$ | Gate oxide thickness |
| $t_{si}$ | Silicon body thickness |
| $t_{BOX}$ | BOX thickness |
| $t_{GP}$ | Ground Plane thickness |
| $d_{GP}$ | Ground Plane Depth |
| $d_{NW}$ | Nanowire Diameter |
| $L_{ext}$ | Source/Drain Extension Length |
| $L_{con}$ | Length of the Control gate |

| | |
|---|---|
| $L_{aux}$ | Length of the Auxiliary gate |
| $L_{con}/L_g$ | Ratio of control gate length to gate length |
| $N_{Sext}$ | Source Extension Doping |
| $N_{Dext}$ | Drain Extension Doping |
| $N_{Channel}$ | Channel Doping |
| $V_{DD}$ | Supply Voltage |
| $V_{th}$ | Threshold Voltage |
| $\phi_{Con}$ | Control gate Work Function |
| $\phi_{aux}$ | Auxiliary gate Work Function |
| 3-D | Three Dimensional |
| $\phi_{M1}$ | Metal 1 Work Function |
| $\phi_{M2}$ | Metal 2 Work Function |