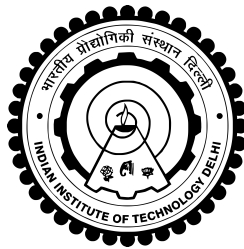


ON-CHIP INSTRUMENTATION TECHNIQUES

AASHISH T R



**Department of Electrical Engineering
Indian Institute of Technology Delhi
May 2025**

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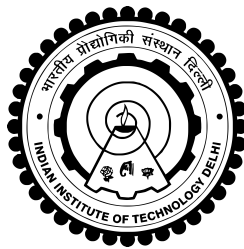
AASHISH T R

Department of Electrical Engineering

Submitted in fulfillment of the requirements
of the degree of

Doctor of Philosophy

to the



Indian Institute of Technology Delhi

May 2025

To my loving *parents*

Certificate

This is to certify that the thesis entitled "**On-Chip Instrumentation Techniques**", being submitted by **Mr. Aashish T R** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by her under my supervision and guidance. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any other degree or diploma.

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Aashish T R

Abstract

Integrated circuits today are built to function at very high frequencies due to the improvement in signal processing bandwidth achieved. Systems such as processors, transceivers, memory sub-systems are designed in extremely scaled-down processes with very fine time resolution to operate at GHz frequencies so as to perform fast and complex functions. This prompts a need for us to build instrumentation systems that can accurately characterize the performance of these complex systems-on-chip. Circuits that are used to probe internal nodes and expose them to pads can degrade the actual performance of the systems, hence triggering a possibility of over-design. This work aims to explore instrumentation systems that can be used for characterization on-chip so that all sensitive performance measurements can be done in-situ. The most preliminary measurements required for accurately estimating performance are voltage, current and time. Multiple systems have been proposed in this work to enable on-chip measurements.

Measuring voltages and currents on a chip requires a reference voltage. In this work, we propose an ultra low power portable reference integrated

regulator that can also support upto 10mA of load current. This system was designed in a TSMC 180nm bulk CMOS process and was able to achieve a temperature stability of $80 \text{ ppm}/^{\circ}\text{C}$ with a core current consumption of 187 pA .

Another suitable candidate for on chip measurement is time and its derivatives, primarily frequency, rise time, fall time etc. To enable these measurements, we propose a state-learning fractional frequency synthesizer with built-in spur reduction. This algorithm is tested using an FPGA development board, discrete DAC and VCO chips. This prototype is used as a proof of concept to show a frequency synthesizer that is fast sweeping (useful for spectrum and s-parameter measurements).

As the PLL works to control the phase noise spectrum within its bandwidth, a VCO with a good spectrum at frequencies outside the bandwidth of the PLL. We propose a new VCO architecture designed at 5GHz that has a figure of merit better than $-200 \text{ dBc}/\text{Hz}/\text{mW}$. The inductors were custom designed and characterized using EMX to achieve better quality factor for the required frequency of operation. The entire VCO with the additional

startup oscillator is designed in the TSMC 65nm LP process. The VCO core consumes about 7mA from a 1.2V supply and has a phase noise of -132 dBc/Hz at a 1 MHz offset.

A common method of observing periodic high frequency signals in the time-domain is by using a sub-sampling oscilloscope. To enable this, we propose a sub-sampling front-end with a low input load of 12 fF followed by a second order continuous time delta sigma ADC. The ADC achieves an approximate ENOB of 12 bits in post-layout extraction and the front-end can track and hold signals upto few GHz.

सारांश

आज के एकीकृत सर्किट बहुत उच्च आवृत्तियों पर कार्य करने के लिए बनाए जाते हैं, जो सिग्नल प्रोसेसिंग बैंडविड्थ में सुधार के कारण संभव हो पाया है। प्रोसेसर, ट्रांसीवर, मेमोरी सब-सिस्टम जैसे सिस्टम अत्यधिक लघु तकनीकी प्रक्रिया में डिज़ाइन किए जाते हैं, जिनमें बहुत ही सूक्ष्म समय संकल्प होता है ताकि वे गीगाहर्ट्ज़ फ्रीक्वेंसी पर तेज़ और जटिल कार्य कर सकें।

इससे यह आवश्यकता उत्पन्न होती है कि हम ऐसे इंस्ट्रूमेंटेशन सिस्टम बनाएं जो इन जटिल सिस्टम-ऑन-चिप के प्रदर्शन को सटीक रूप से माप सकें। जो सर्किट आंतरिक नोड्स की जांच के लिए उपयोग किए जाते हैं और उन्हें पैड्स से जोड़ते हैं, वे सिस्टम के वास्तविक प्रदर्शन को कम कर सकते हैं, जिससे ओवर-डिज़ाइन की संभावना बढ़ जाती है। यह कार्य ऑन-चिप मापन की सुविधा प्रदान करने वाले इंस्ट्रूमेंटेशन सिस्टम्स की खोज पर केंद्रित है ताकि संवेदनशील प्रदर्शन माप इन-सिटू ही किए जा सकें।

प्रदर्शन का सटीक अनुमान लगाने के लिए आवश्यक सबसे बुनियादी माप हैं: वोल्टेज, करंट और समय। इस कार्य में ऑन-चिप मापन को सक्षम बनाने के लिए कई सिस्टम्स प्रस्तावित किए गए हैं।

चिप पर वोल्टेज और करंट मापने के लिए एक रेफरेंस वोल्टेज की आवश्यकता होती है। इस कार्य में, हमने एक अल्ट्रा-लो पावर पोर्टेबल रेफरेंस इंटिग्रेटेड रेगुलेटर प्रस्तावित किया है जो 10mA तक के लोड करंट को भी सपोर्ट कर सकता है। यह सिस्टम TSMC 180nm बल्क CMOS प्रक्रिया में डिज़ाइन किया गया है और यह 80 ppm/°C तापमान स्थिरता और 187 pA के कोर करंट खपत के साथ कार्य करता है।

समय और उसके व्युत्पन्न जैसे फ्रीक्वेंसी, राइज़ टाइम, फॉल टाइम आदि ऑन-चिप मापन के लिए अन्य उपयुक्त मानदंड हैं। इन्हें सक्षम बनाने के लिए, हमने बिल्ट-इन स्पर रिडक्शन के साथ एक स्टेट-लर्निंग

फ्रैक्शनल फ्रीक्वेंसी सिंथेसाइज़र प्रस्तावित किया है। इस एल्गोरिदम का परीक्षण FPGA डेवलपमेंट बोर्ड, डिस्क्रीट DAC और VCO चिप्स के साथ किया गया है। यह प्रोटोटाइप एक फास्ट स्वीपिंग फ्रीक्वेंसी सिंथेसाइज़र के कॉन्सेप्ट का प्रमाण प्रदान करता है, जो स्पेक्ट्रम और S-पैरामीटर मापन में उपयोगी होता है।

जैसे ही PLL अपने बैंडविड्थ के भीतर फेज़ नॉइज़ स्पेक्ट्रम को नियंत्रित करता है, वैसे ही PLL की बैंडविड्थ के बाहर अच्छी स्पेक्ट्रल विशेषताओं वाला VCO आवश्यक होता है। हमने 5GHz पर डिज़ाइन की गई एक नई VCO आर्किटेक्चर प्रस्तावित की है, जिसका फिगर ऑफ मेरिट -200 dBc/Hz/mW से बेहतर है। आवश्यक ऑपरेटिंग फ्रीक्वेंसी के लिए बेहतर क्वालिटी फैक्टर प्राप्त करने हेतु इंडक्टर्स को EMX के माध्यम से कस्टम डिज़ाइन और कैरेक्तराइज़ किया गया है। पूरा VCO, स्टार्टअप ऑस्सीलेटर सहित, TSMC 65nm LP प्रक्रिया में डिज़ाइन किया गया है। VCO कोर लगभग 7mA करंट का 1.2V सप्लाइ से उपभोग करता है और 1 MHz ऑफसेट पर -132 dBc/Hz फेज़ नॉइज़ देता है।

उच्च आवृत्ति की आवर्ती संकेतों को टाइम-डोमेन में देखने की एक सामान्य विधि है सब-सैंपलिंग ऑसिलोस्कोप का उपयोग करना। इसे सक्षम करने के लिए, हमने 12 fF के निम्न इनपुट लोड वाले एक सब-सैंपलिंग फ्रंट-एंड का प्रस्ताव रखा है, जिसके बाद एक सेकंड ऑर्डर कंटीन्युअस टाइम डेल्टा सिग्मा ADC है। यह ADC पोस्ट-लेआउट एक्सट्रैक्शन में लगभग 12 बिट्स का ENOB प्राप्त करता है और फ्रंट-एंड कुछ GHz तक के संकेतों को ट्रैक और होल्ड कर सकता है।

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