

# **FlexDFD: FLEXIBLE DFD HARDWARE FOR EFFICIENT POST-SILICON VALIDATION**

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# **FlexDFD: FLEXIBLE DFD HARDWARE FOR EFFICIENT POST-SILICON VALIDATION**

by

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# Certificate

This is to certify that the thesis titled **FlexDFD: Flexible DFD Hardware for Efficient Post-Silicon Validation** being submitted by **C. Sandeep** for the award of **Doctor of Philosophy** in **Department of Computer Science and Engineering** is a record of bona-fide work carried out by him under our guidance and supervision at the **Department of Computer Science and Engineering, Indian Institute of Technology Delhi**. The work presented in this thesis has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma.

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# Abstract

*The increasing complexity of designs have rendered traditional pre-silicon verification strategies inadequate, as a result of which, an increasing number of functional errors are escaping into silicon. Post-silicon validation has emerged as a viable solution to this problem, where initial samples of the chip are tested in an environment that resembles its intended operating conditions. The foremost challenge during post-silicon validation is the limited visibility into the functioning of the chip. Two approaches have been proposed to tackle this: (i) capture atomic snapshots of the state at regular intervals, and (ii) record the behavior of a few internal signals continuously. The data thus captured through either of the approaches is transferred off-chip for further analysis to detect the presence of bugs. Such off-chip transfers are usually over a low bandwidth debug link, which makes them extremely time-consuming.*

*In this thesis, we propose techniques to minimize the time taken for such transfers under both the aforementioned approaches by discarding as much redundant or irrelevant data as is possible in order to reduce the volume of data to be transferred off-chip. Under the first approach, we achieve this by only transferring the changes to the state since the previous snapshot. We propose a novel hardware structure called Interval Table that stores the information on updates to the state using negligible area. Under the second approach, we propose novel hardware to summarize the behavior of the internal signals by discarding the information that is irrelevant to debug the observed error.*

*Further, instead of disabling the on-chip debug hardware, we propose to reuse them in-field in ways that benefit the target applications. We demonstrate this through an example where the proposed summarizer is reprogrammed to function as a jitter unit that helps mitigate operating system jitter.*

## संक्षेप

डिजाइनों की बढ़ती जटिलता के कारण पारंपरिक पूर्व-सिलिकॉन सत्यापन रणनीति अपर्याप्त है, जिसके परिणामस्वरूप, सिलिकॉन में कार्यात्मक त्रुटियों की संख्या बढ़ रही है। पोस्ट-सिलिकॉन सत्यापन इस समस्या का एक व्यवहार्य समाधान के रूप में उभरा है, जहां चिप के शुरुआती नमूनों का परीक्षण एक ऐसे वातावरण में किया जाता है, जो इसकी प्रयुक्त परिस्थितियों के अनुरूप होता है। पोस्ट-सिलिकॉन सत्यापन के दौरान सबसे बड़ी चुनौती चिप की कार्य पद्धति में सीमित दृश्यता है। इस से निपटने के लिए दो तरीकों का प्रस्ताव दिया गया है: (i) नियमित अंतराल पर चिप की आंतरिक अवस्था को कैप्चर करना, और (ii) लगातार कुछ आंतरिक संकेतों का व्यवहार रिकॉर्ड करना। इस तरह से लिया डेटा, बग की उपस्थिति का पता लगाने के लिए आगे विश्लेषण के लिए ऑफ-चिप स्थानांतरित किया जाता है। ऐसे ऑफ-चिप स्थानान्तरण आमतौर पर कम बैंडविड्थ वाले डीबग लिंक के दरिये होता है, जो इसे समय-उपभोक्ता बना देता है।

इस थीसिस में, हम पूर्वकथित तरीकों के तहत डेटा को ऑफ-चिप स्थानांतरित करने के लिए लिया गया समय कम करने की तकनीक का प्रस्ताव करते हैं। पहले तकनीक के अंतर्गत, हम केवल पिछले स्नैपशॉट के बाद से आंतरिक अवस्था में हुई परिवर्तनों को स्थानांतरित करते हैं। हम 'अंतराल तालिका' नामक एक नया हार्डवेयर संरचना का प्रस्ताव करते हैं जो नगण्य क्षेत्र का उपयोग करते हुए आंतरिक अवस्था में हुई परिवर्तनों की जानकारी संग्रहीत करता है। दूसरे तकनीक के तहत, हम उस सूचना को छोड़कर आंतरिक संकेतों के व्यवहार को सारांशित करने के लिए नया हार्डवेयर का प्रस्ताव देते हैं जो त्रुटि को डिबग करने के लिए अनुपयोगी है।

इसके अलावा, ऑन-चिप डिबग हार्डवेयर को अक्षम करने के बजाय, हम इन्को दोबारा इन-फील्ड उपयोग करने का नये तरीकों का प्रस्ताव करते हैं जिससे अनुप्रयोगों को लाभ पहुंचाती हैं। हम इसे एक उदाहरण के माध्यम से दर्शाते हैं।

# Contents

<b>List of Figures</b>	<b>v</b>
<b>List of Tables</b>	<b>vii</b>
<b>1 Introduction</b>	<b>1</b>
1.1 Literature survey . . . . .	4
1.1.1 Behavior Capturing Techniques . . . . .	6
1.1.2 Behavior Analysis techniques . . . . .	20
1.1.3 Component Specific Solutions . . . . .	24
1.2 Thesis Outline . . . . .	28
1.2.1 Goal . . . . .	28
1.2.2 Proposal 1 - Area-aware Update Trackers . . . . .	29
1.2.3 Proposal 2 - Trace Summarizer . . . . .	29
1.2.4 Proposal 3 - In-field Reuse of DFD Hardware . . . . .	30
<b>2 Area-aware state-capturing scheme</b>	<b>33</b>
2.1 Methodology – Shared Cache . . . . .	35
2.1.1 Definitions . . . . .	35
2.1.2 <b>Brute-force method: t-lines/bit bit-vector</b> . . . . .	36
2.1.3 Interval Table . . . . .	37
2.1.4 Offline Algorithm (Optimal) . . . . .	39
2.1.5 <b>Online Algorithm 1: Greedy Heuristic</b> . . . . .	40
2.1.6 <b>Online Algorithm 2: Hybrid Scheme</b> . . . . .	44
2.2 Methodology – Distributed Caches . . . . .	46
2.2.1 Horizontal Sharing . . . . .	47
2.2.2 Vertical Sharing . . . . .	48
2.3 Hardware Design . . . . .	49

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2.3.1	Sorted Storage of Intervals . . . . .	49
2.3.2	Memory Configuration . . . . .	50
2.3.3	Logic Design . . . . .	50
2.3.4	Update Buffer . . . . .	52
2.3.5	Extensions for Hybrid Algorithm . . . . .	52
2.4	Experiments . . . . .	53
2.4.1	Setup . . . . .	53
2.4.2	Overhead of various schemes – Shared Cache . . . . .	54
2.4.3	Overhead of various schemes – Distributed Caches . . . . .	57
2.4.4	Update Buffer Size vs. Processor stalls – Shared Cache . . . . .	62
2.4.5	Update Buffer Size vs. Processor stalls – Distributed Caches . . . . .	65
2.4.6	Area Overhead . . . . .	65
2.4.7	Power Overhead . . . . .	67
2.4.8	Summary . . . . .	67
2.5	Chapter Summary . . . . .	67
<b>3</b>	<b>Trace conditioning using Summaries</b>	<b>69</b>
3.1	Trace Summaries . . . . .	73
3.1.1	Background . . . . .	73
3.1.2	Storage Specification Language (SSL) . . . . .	75
3.1.3	Spatial Summary . . . . .	77
3.1.4	Temporal Summary . . . . .	78
3.2	Architectural considerations . . . . .	81
3.2.1	Tapered storage . . . . .	81
3.2.2	Split Architecture . . . . .	82
3.2.3	Unified Architecture . . . . .	83
3.2.4	Overlapped Architecture . . . . .	84
3.3	Hardware Design . . . . .	85

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3.3.1	Spatial Summarizer . . . . .	86
3.3.2	Temporal Summarizer . . . . .	89
3.3.3	Programming the Summarizer . . . . .	93
3.3.4	Limitations . . . . .	94
3.4	Extensions to distributed and multi-core systems . . . . .	95
3.4.1	Specification . . . . .	96
3.4.2	Storage Architecture . . . . .	97
3.4.3	Hardware extensions . . . . .	98
3.5	Experiments . . . . .	98
3.5.1	Setup . . . . .	98
3.5.2	Bug Scenarios . . . . .	99
3.5.3	Area Overhead . . . . .	105
3.6	Chapter Summary . . . . .	106
<b>4</b>	<b>Reusing DFD hardware</b>	<b>107</b>
4.1	Extensions for Reusability . . . . .	108
4.2	Summarizer as Jitter Units . . . . .	111
4.2.1	Background . . . . .	111
4.2.2	Design of Dedicated Jitter Units . . . . .	115
4.2.3	Summarizer as a Jitter Unit . . . . .	121
4.2.4	Limitations of Reuse . . . . .	123
4.2.5	Experiments . . . . .	124
4.3	Chapter summary . . . . .	128
<b>5</b>	<b>Conclusions and Future Work</b>	<b>129</b>
5.1	Future Directions of Research . . . . .	130
	<b>References</b>	<b>135</b>

# List of Figures

1.1	Development life cycle with post-silicon validation . . . . .	2
1.2	Flow of post-silicon validation . . . . .	5
1.3	Classification of post-silicon validation methodologies . . . . .	5
1.4	Illustration of state-dump methodology . . . . .	8
2.1	Example of a Bit-vector with corresponding 2-lines/bit bit-vector. . . . .	36
2.2	Interval merging decisions for $k = 2$ . . . . .	38
2.3	Illustration of the optimal Offline algorithm (a) Initial Gap Table (b) Sorted Gap Table (c) Optimal Interval Table for $k = 2$ (d) Optimal Interval Table for $k = 3$ . . . . .	40
2.4	(a) Illustration of local gaps and global gaps (b) Final bit-vector on accommodating new incoming request . . . . .	42
2.5	Illustration of Greedy algorithm when $minGlobalGap$ is smaller than $minLocalGap$ . . . . .	43
2.6	Working of the Hybrid algorithm . . . . .	45
2.7	Horizontal Sharing scheme for Distributed caches . . . . .	47
2.8	Vertical Sharing scheme for Distributed caches . . . . .	49
2.9	Hardware design of Greedy algorithm . . . . .	51
2.10	<i>Overhead</i> of proposed algorithms for different $k$ (shared cache) . . . . .	56
2.11	<i>Overhead</i> of t-lines/bit bit-vector – shared cache . . . . .	58
2.12	<i>Overhead</i> of a simple bit-vector during horizontal sharing (distributed cache) . . . . .	59
2.13	<i>Overhead</i> of proposed algorithms for different $k$ (distributed cache) . . . . .	60
2.14	Slowdown vs. Buffer Size (shared cache) . . . . .	63
2.15	Slowdown vs. Buffer Size (distributed cache) . . . . .	64

3.1	High-level schematic of proposed scheme. (a) Trace buffer organized as a circular queue. (b) Flexible partition (created at runtime) of the circular queue into Detailed and Summary Buffers. . . . .	72
3.2	Trace messages stored by various schemes. The vertical axis represents time, and blocks numbered 1-7 represent the logical fields within a trace message. The colored blocks represent the fields within trace messages that are stored into the trace buffer by: (a) event triggers, (b) spatial summary, (c) temporal summary, (d) a combination of spatial and temporal summaries, (e) captured contents of (d) is compressed further. . . . .	74
3.3	Split architecture . . . . .	82
3.4	Unified architecture . . . . .	83
3.5	Overlapped architecture . . . . .	84
3.6	High-level design of Trace Summarizer (for the Overlapped architecture)	85
3.7	High-level design of our proposed Spatial Summarizer on the LEON3 processor . . . . .	86
3.8	Design of the Online Filter . . . . .	87
3.9	Illustration of working of the Online Filter . . . . .	88
3.10	Design of the Temporal Summarizer . . . . .	89
3.11	Design of Boolean Expression Tree . . . . .	91
3.12	Design of a boolean expression evaluator node . . . . .	91
3.13	Design of a distributed storage architecture . . . . .	97
4.1	Extensions to the summarizer for in-field reuse . . . . .	109
4.2	Illustration of jitter (signal-wait scenario) . . . . .	113
4.3	Design of the jitter unit (One per core) . . . . .	115
4.4	Time overhead (Splash2 & Parsec) . . . . .	126
4.5	Frequency across subframes for water_spatial, and facesim . . . . .	127

# List of Tables

2.1	Number of cache lines transferred off-chip for shared caches . . . . .	57
2.2	Number of cache lines transferred off-chip for distributed caches . . . . .	61
2.3	Area overhead – Shared cache . . . . .	66
3.1	Fields in instruction trace of LEON3 SoC . . . . .	73
3.2	Details of traces generated by the DFD hardware . . . . .	99
3.3	Number of stalls required for different trace buffer configurations when storing spatial summaries . . . . .	101
3.4	Area overhead of the proposed DFD hardware . . . . .	106
4.1	Simulation Setup . . . . .	125