DESIGN, CONTROL AND DEVELOPMENT OF SINGLE PHASE MULTILEVEL CONVERTERS FOR PV BASED GRID-TIED APPLICATIONS

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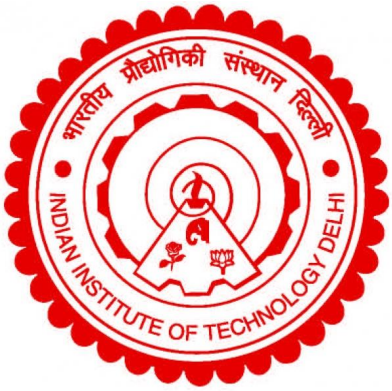

DEPARTMENT OF ELECTRICAL ENGINEERING

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DESIGN, CONTROL AND DEVELOPMENT OF SINGLE PHASE MULTILEVEL CONVERTERS FOR PV BASED GRID-TIED APPLICATIONS

by

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in fulfilment of the requirements of the degree of Doctor of Philosophy

to the

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Dedicated to

My family and all the teachers whom I came across at different stages during my life.

CERTIFICATE

It is certified that the thesis entitled "**Design, Control and Development of Single Phase Multilevel Converters for PV Based Grid-Tied Applications**," being submitted by **Mrs. Nidhi Mishra** for award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of the student work carried out by her under my supervision and guidance. The matter embodied in this thesis, has not been submitted for the award of any other degree or diploma.

Dated: September 22, 2020

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ABSTRACT

Multilevel converters (MLCs) are capable of providing power transfer at lower harmonics distortion, reduced switching stresses, less electromagnetic interference, and minimum filter size. The multilevel inverters increase the voltage to a level above than rating of semiconductor switches by connecting them in suitable arrangement. A high voltage stepped wave closer to a pure sine wave is main motive of bringing such multilevel converters. Various topologies like neutral point clamped (NPC) converter, cascaded H bridge (CHB) converter and flying capacitor (FC) are available in the literature. Higher number of levels provide above-mentioned advantages but at the cost of an increase in converter structure. The system must be compact and cost-effective to be accepted in the practical system. Various low switching frequency based medium voltage multilevel converters are implemented to adhere with minimum switching losses and keeping harmonic standards in an acceptable limit. A major disadvantage of conventional topologies, is that switches are increased drastically increasing controller complexity, switching losses, and financial burden. Hence, moving towards reduced number of semiconductor switches, DC-link capacitors, flying capacitors, and clamped diodes to cater such issues, various topologies have come up in the field of multilevel converters. The CHB configurations with symmetric and asymmetric sources are investigated for five and seven-level grid-connected PV array fed applications. A prototype of five-level CHB is implemented and its performance is analyzed at variable irradiances and abnormal conditions using solar PV emulators. Moreover, NPC and active NPC topologies with neutral point voltage balancing and flying capacitor control have been incorporated in this work. Furthermore, packed U-cell (PUC) topologies for seven, eleven and fifteen level output voltage, are presented for closed loop solar photovoltaic grid-tied applications. The modified PUC with voltage boost mode capability is investigated in closed-loop system and input DC sources need not be higher than PCC voltage. An eight switch eleven level reduced switch count topology is one of the main contribution of the thesis. A new topology with twenty-five level output voltage generation with twelve active switches is incorporated in the work for solar photovoltaic grid-tied applications. Moreover, a nearest level

modulation strategy is incorporated to achieve fundamental switching and minimum switching losses. The multiple topologies are covered in closed-loop single-phase single stage grid-connected configurations. The incremental conductance (INC) and perturb and observe maximum power point techniques are implemented within the inverter control to have single-stage configuration. The efficiency of single-stage makes it more viable as compared to extra boost conversion stage in double stage configurations. The power quality indices are worked and results are found compliant with the IEEE 519 and IEEE 61727 standards. Moreover, real-time testing of such topologies is executed using rapid prototyping based digital simulators. Few topologies are run in RT-LAB environment at physical clock time in hardware synchronization mode. Moreover, some topologies are simulated using MATLAB/Simulink and results are validated using hardware laboratory setup and in hardware in loop (HIL) using OPALRT real-time digital simulator (RTDS). These systems are evaluated in terms of cost-effectiveness, reduced switch count, power quality standards, simplicity, robust control, and practical feasibility.

सार

मल्टीलेवल कन्वर्टर्स (MLC) कम हार्मोनिक्स विरूपण, कम स्विचिंग तनाव, कम विद्युत चुम्बकीय हस्तक्षेप और न्यूनतम फ़िल्टर आकार में बिजली हस्तांतरण प्रदान करने में सक्षम हैं। बहुस्तरीय इनवर्टर उपयुक्त व्यवस्था में कनेक्ट करके सेमीकंडक्टर स्विच की रेटिंग की तुलना में ऊपर के स्तर तक वोल्टेज बढ़ाते हैं। शुद्ध साइन लहर के करीब एक उच्च वोल्टेज की लहर ऐसी बहुस्तरीय कन्वर्टर्स को लाने का मुख्य उद्देश्य है। न्यूट्रल पॉइंट क्लैंपेड (NPC) कनवर्टर, कैस्केड एच ब्रिज (CHB) कनवर्टर और फ्लाइंग कैपेसिटर (FC) जैसी विभिन्न टोपोलॉजी साहित्य में उपलब्ध हैं। स्तरों की उच्च संख्या उपर्युक्त फायदे प्रदान करती है लेकिन कनवर्टर संरचना में वृद्धि की कीमत पर। व्यावहारिक प्रणाली में स्वीकार किए जाने के लिए प्रणाली को कॉम्पैक्ट और लागत प्रभावी होना चाहिए। न्यूनतम स्विचिंग नुकसान और एक स्वीकार्य सीमा में हार्मोनिक मानकों को ध्यान में रखते हुए विभिन्न कम स्विचिंग आवृत्ति आधारित मध्यम वोल्टेज मल्टीलेवल कन्वर्टर्स को लागू किया जाता है। पारंपरिक टोपोलॉजी का एक बड़ा नुकसान यह है कि स्विच तेजी से नियंत्रक जटिलता को बढ़ा रहे हैं, स्विचिंग घाटे और वित्तीय बोझ को बढ़ाते हैं। इसलिए, इस तरह के मुद्दों को पूरा करने के लिए सेमीकंडक्टर स्विच, डीसी-लिंक कैपेसिटर, फ्लाइंग कैपेसिटर और क्लैंप किए गए डायोड की कम संख्या की ओर बढ़ते हुए, मल्टीलेवल कन्वर्टर्स के क्षेत्र में विभिन्न टोपोलॉजी सामने आई हैं। सममित और असममित स्रोतों के साथ सीएचबी कॉन्फ़िगरेशन की जांच पांच और सात-स्तरीय ग्रिड-कनेक्टेड पीवी सरणी खिलाए गए अनुप्रयोगों के लिए की जाती है। पांच-स्तरीय सीएचबी का एक प्रोटोटाइप लागू किया गया है और इसके प्रदर्शन का विश्लेषण सौर विकिरण और असामान्य परिस्थितियों में सौर पीवी एमुलेटर का उपयोग करके किया गया है। इसके अलावा, एनपीसी और सक्रिय एनपीसी टोपोलॉजी तटस्थ बिंदु वोल्टेज संतुलन और उड़ान संधारित्र नियंत्रण के साथ इस काम में शामिल किया गया है। इसके अलावा, सात, ग्यारह और पंद्रह स्तर के आउटपुट वोल्टेज के लिए पैक्ड यू-सेल (पीयूसी) टोपोलॉजी बंद लूप सौर फोटोवोल्टिक ग्रिड-बंधे अनुप्रयोगों के लिए प्रस्तुत किए जाते हैं। वोल्टेज-बूस्ट मोड क्षमता के साथ संशोधित पीयूसी को बंद-लूप सिस्टम में जांच की जाती है और इनपुट डीसी स्रोतों को पीसीसी वोल्टेज से अधिक नहीं होना चाहिए। एक आठ स्विच ग्यारह स्तर कम स्विच गिनती टोपोलॉजी थीसिस के मुख्य योगदान में से एक है। सोलर

फोटोवोल्टिक ग्रिड-बंधे हुए अनुप्रयोगों के लिए बारह सक्रिय स्विच के साथ पच्चीस स्तरीय आउटपुट वोल्टेज पीढ़ी के साथ एक नई टोपोलॉजी को काम में शामिल किया गया है। इसके अलावा, मौलिक स्विचिंग और न्यूनतम स्विचिंग नुकसान को प्राप्त करने के लिए एक निकटतम स्तर की मॉड्यूलेशन रणनीति शामिल की गई है। कई टोपोलॉजी बंद लूप सिंगल-फेज सिंगल स्टेज ग्रिड-कनेक्टेड कॉन्फ़िगरेशन में शामिल हैं। वृद्धिशील चालन (INC) और गड़बड़ी और निरीक्षण करते हैं अधिकतम शक्ति बिंदु तकनीकों को सिंगल-स्टेज कॉन्फ़िगरेशन के लिए इन्वर्टर नियंत्रण के भीतर कार्यान्वित किया जाता है। सिंगल-स्टेज की दक्षता डबल स्टेज कॉन्फ़िगरेशन में अतिरिक्त बढ़ावा रूपांतरण चरण की तुलना में इसे अधिक व्यवहार्य बनाती है। बिजली की गुणवत्ता के सूचकांक पर काम किया जाता है और परिणाम IEEE 519 और IEEE 61727 मानकों के अनुरूप पाए जाते हैं। इसके अलावा, रैपिड प्रोटोटाइप आधारित डिजिटल सिमुलेटर का उपयोग करके इस तरह की टोपोलॉजी का वास्तविक समय परीक्षण निष्पादित किया जाता है। हार्डवेयर सिंक्रनाइज़ेशन मोड में भौतिक घड़ी के समय आरटी-एलएबी वातावरण में कुछ टोपोलॉजी चलाए जाते हैं। इसके अलावा, कुछ टोपोलॉजी MATLAB / Simulink का उपयोग करके सिम्युलेटेड हैं और परिणाम OPALRT वास्तविक समय डिजिटल सिम्युलेटर (RTDS) का उपयोग करके हार्डवेयर प्रयोगशाला सेटअप और लूप (HIL) में हार्डवेयर का उपयोग करके मान्य किए जाते हैं। इन प्रणालियों का मूल्यांकन लागत-प्रभावशीलता, कम स्विच काउंट, बिजली की गुणवत्ता मानकों, सादगी, मजबूत नियंत्रण और व्यावहारिक व्यवहार्यता के संदर्भ में किया जाता है।

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OFABBREVIATIONS

MLC	Multilevel Converters
CHB	Cascaded H-Bridge
NPC	Neutral Point Clamped
PUC	Packed U-Cell
THD	Total Harmonic Distortion
ANPC	Active Neutral Point Clamped
FC	Flying Capacitors
IGBT	Insulated Gate Bipolar Transistors
PCC	Point of Common Coupling
SPV	Solar Photovoltaic
TDD	Total Demand Distortion
PWM	Pulse Width Modulation
MPPT	Maximum Power Point Tracking
INC	Incremental Conductance
LQI	Linear Quadratic Integral
SLCHBC	Seven Level Cascaded H-Bridge Converter
LS-PWM	Level Shifted Pulse Width Modulation
FLMPUC	Five Level Modified Packed U Cell Converter
SLMPUC	Seven Level Modified Packed U Cell Switched Converter
NPV	Neutral Point Voltage
PS-PWM	Phase-Shifted Pulse Width Modulation
CPUC	Cascaded Packed U Cell
NLMT	Nearest Level Modulation Technique