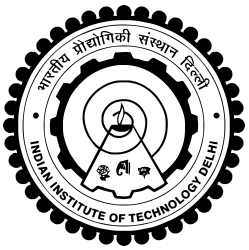
THE EIGENANT ALGORITHM: EXTENSIONS, APPLICATIONS AND HARDWARE IMPLEMENTATION

UDIT KUMAR



DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY DELHI

OCTOBER 2016

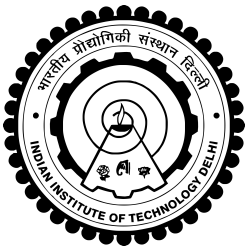
©Indian Institute of Technology Delhi (IITD), New Delhi, 2016

THE EIGENANT ALGORITHM: EXTENSIONS, APPLICATIONS AND HARDWARE IMPLEMENTATION

by

UDIT KUMAR
Department of Electrical Engineering

Submitted
in fulfillment of the requirements of the degree of Doctor of Philosophy
to the



Indian Institute of Technology Delhi
OCTOBER 2016

Certificate

This is to certify that the thesis entitled **"The EigenAnt Algorithm: Extensions, Applications and Hardware Implementation"**, being submitted by **Mr. Udit Kumar** for the award of the degree of **Doctor of Philosophy** to the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under our supervision and guidance. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any other degree or diploma.

Dr. Jayadeva
Professor
Department of Electrical Engineering,
Indian Institute of Technology Delhi,
Hauz Khas, New Delhi - 110016,
INDIA.

Dr. Kaushik Saha
Co-supervisor
Chief Technology Officer,
Samsung R&D Institute India - Delhi,
2A, Sector - 126, Noida,
Uttar Pradesh - 201303, INDIA.

Acknowledgments

I would like to express my greatest gratitude to my supervisors Prof. Jayadeva and Dr. Kaushik Saha for their guidance, interest, advice, support and help throughout the course of the present work. I am grateful for having the opportunity to work with them and hope that I shall continue to have their blessings in the future. I am also indebted to my research committee members, Prof. Santanu Chaudhury, Prof. Amit Kumar and Dr. Shouri Chatterjee for their valuable insights during my research work. Dr. Shouri Chatterjee's help in chip fabrication and PCB design requires special mention.

I am grateful to the faculty and staff at the Department of Electrical Engineering at the Indian Institute of Technology Delhi for providing me an excellent work environment during the past years. I wish to acknowledge the funding provided by Department of Science and Technology under the project "Efficient Algorithms for Global Optimization and for Learning and their Hardware Implementation" for chip manufacturing. I am grateful to Natronix Semiconductor Technology (formerly SPEL Semiconductor Limited) for helping me with their expertise on chip packaging. Rajesh Gupta and Madhur Kashyap's help in chip tape-out has been instrumental. I would also like to acknowledge the help which Mr. Rakesh Kumar, Mukesh Singh, Ritwick Pahari provided me during my research work.

I would like to thank the students who made my experience at IIT Delhi a memorable one. Words fail me to express my deepest thanks to Sumit Soman for being a great friend, his cooperation helped me to reach this milestone. I enjoyed working with Pawas, Munish, Aashish, Rajshree, Kinde, Roohie, Gajendranath, Manpreet, Navneet and others. I would also like to thank my former employer, STMicroelectronics, the management and my colleagues there for their support, particularly Olivier Florent and Bhanu Prakash. I am also grateful to my present employer Atrenta India Pvt. Ltd.

This thesis would not have been possible without the help and unconditional support offered by my family. I am truly grateful to my parents, sisters, wife and son, who have stood by me in all times.

Udit Kumar

Abstract

Biological phenomena prevalent in nature and among organisms have inspired development of algorithms for self-organization in dynamic scenarios. The behavior of ants has been found to particularly suit tasks such as optimization, and this has been modeled as the class of Ant Colony Optimization (ACO) algorithms. This has primarily been motivated by the fact that ants travelling from a source node (nest) to a destination node (food source) deposit pheromone on the path traversed, and over time the paths traversed by the ants converge to the shortest path, which represents the stabilized system at equilibrium. Eventually, all ants end up choosing the shortest path as it has the highest pheromone concentration.

One can analogously simulate this scenario for solving several optimization tasks, and expect a similar behavior to eventually lead to finding an optimal path (or solution). Though this has been the thrust of most of the ACO-based optimization approaches, a variant called the EigenAnt has been the first to have a mathematical proof of convergence. This thesis explores extensions, applications and hardware realization of the EigenAnt algorithm to illustrate its widespread practical applicability.

The initial chapters establish the EigenAnt as an algorithm of choice for discrete and continuous optimization tasks. There are a plethora of tasks that involve optimization. The use of EigenAnt based approaches for these tasks helps attain better solutions to the problems, often with lower computational cost. Applications include problems involving the optimization of discrete variables as well as others that employ continuous valued variables. The inferences lead to conclude that the biological phenomena of traversal of ants indeed benefits optimization routines, irrespective of the nature of the variables involved.

The true prospective benefits of such biologically inspired algorithms can be gauged only when they are implemented in hardware. This enables such approaches to be run with data generated from natural sources, which is crucial to evaluate its practical benefit. An additional aspect that stems from hardware implementation is the choice of optimal

design architecture in terms of design area and power consumption that would enable these algorithms to be used efficiently despite limited precision or accuracy. Hardware implementation imposes constraints on the algorithm that can potentially alter its behaviour and needs careful study. The sequel focuses on determining the effect of quantization on algorithm behavior. This is with a view to understanding the effect of precision during floating to fixed-point conversion for hardware implementation of EigenAnt. It is shown that for the case of the EigenAnt, a feasible architecture is possible, and the same has been implemented on a VLSI ASIC that was fabricated in a 180 nm CMOS process.

Contents

List of Figures

List of Tables