LEVERAGING SILICON NANOPHOTONICS FOR ON-CHIP AND OFF-CHIP COMMUNICATION

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by

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Certificate

This is to certify that the thesis titled **LEVERAGING SILICON NANOPHOTONICS FOR ON-CHIP AND OFF-CHIP COMMUNICATION** being submitted by **Mr. Janibul Bashir** for the award of **Doctor of Philosophy** in Computer Science and Engineering is a record of bona fide work carried out by him under my guidance and supervision at the Department of Computer Science and Engineering, Indian Institute of Technology Delhi. The work presented in this thesis has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma.

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Abstract

Numerous challenges present themselves when scaling traditional on-chip electrical networks to large many-core processors. Some of these challenges include high latency, limitations on bandwidth, and power consumption. Researchers have, therefore, been looking for alternatives. As a result, on-chip nanophotonics has emerged as a strong substitute for traditional electrical NoCs. However, optical networks are not a panacea to all our problems. They still have significant issues with respect to high static power consumption and scalability.

In this work, we propose various techniques to decrease the static power consumption in on-chip optical interconnects. We start by proposing two novel techniques to reduce static power consumption in photonic on-chip networks – a neural network based method for laser modulation by predicting optical traffic, and a distributed and altruistic algorithm for channel sharing – that are significantly closer to a theoretically ideal scheme. In spite of this, a lot of laser power still gets wasted. We propose to reuse this energy to heat micro-ring resonators (achieve thermal tuning) by efficiently recirculating it. These three methods help us significantly reduce the energy requirements.

However, area and manufacturing yield restrict such designs to single chips with small number of cores (16-32). As a result, we propose a scalable photonic based multi-chip architecture by leveraging the non-uniform cache architecture (NUCA) scheme on top of a virtual chip in order to decrease inter chip communication and increase the hit rate in the last level cache.

After that we proceed to improve the performance of GPUs with the help of silicon nanophotonics. We propose an energy efficient and scalable optical interconnect for GPUs. We intelligently divide the components in a GPU into different types of clusters and enable these clusters to communicate optically with each other. In order to reduce the network delay, we use separate networks for coherence and non-coherence traffic. Moreover, to reduce the static power consumption in optical interconnects, we modulate the off-chip light source by proposing a novel GPU specific prediction scheme for predicting on-chip network traffic.

Finally, we highlight the fact that unless security concerns are addressed, it will not be possible for third-party vendors to sell optical communication solutions at a large scale. As a result, we proposed a novel, secure, and efficient optical network that is immune to eavesdropping, spoofing, replay, and message-removal attacks. We leveraged some properties of optical networks to bring the expensive cryptographic operations out of the critical path in order to limit the overheads associated with our scheme.

सार

पारंपरिक ऑन-चिप विद्युत नेटवर्क को बड़े-कोर प्रोसेसर में स्केल करते समय कई चुनौतियां खुद को प्रस्तुत करती हैं। इनमें से कुछ चुनौतियों में उच्च विलंबता, बैंडविड्थ पर सीमाएं और बिजली की खपत शामिल हैं। इसलिए, शोधकर्ताओं ने विकल्प की तलाश की है। नतीजतन, ऑन-चिप नेनोफोटोनिक्स पारंपरिक विद्युत एनओसीएस के लिए एक मजबूत विकल्प के रूप में उभरा है। हालाँकि, ऑप्टिकल नेटवर्क हमारी सभी समस्याओं के लिए रामबाण नहीं हैं। उच्च स्थिर बिजली की खपत और मापनीयता के संबंध में उनके पास अभी भी महत्वपूर्ण मुद्दे हैं। इस काम में, हम ऑनचिप ऑप्टिकल इंटरकनेक्ट में स्थैतिक बिजली की खपत को कम करने के लिए विभिन्न तकनीकों का प्रस्ताव करते हैं। हम फोटोनिक ऑन-चिप नेटवर्क में स्थैतिक बिजली की खपत को कम करने के लिए दो उपन्यास तकनीकों का प्रस्ताव करके शुरू करते हैं - ऑप्टिकल ट्रैफिक की भविष्यवाणी करके लेजर मॉड्यूलेशन के लिए एक तंत्रिका नेटवर्क आधारित विधि, और चैनल साझा करने के लिए एक वितरित और परोपकारी एल्गोरिथ्म - जो सैद्धांतिक रूप से आदर्श के करीब हैं योजना। इसके बावजूद, लेज़र की बहुत सी शक्ति अभी भी बर्बाद हो जाती है। हम माइक्रो-रिंग रेज़ोनेटर (थर्मल ट्यूनिंग को प्राप्त करने) को कुशलतापूर्वक पुन: प्रसारित करके इस ऊर्जा का पुन: उपयोग करने का प्रस्ताव करते हैं। ये तीन विधियां हमें ऊर्जा आवश्यकताओं को कम करने में मदद करती हैं। हालांकि, क्षेत्र और विनिर्माण उपज इस तरह के डिजाइनों को कम संख्या में कोर (सोलह-बत्तीस) के साथ एकल चिप्स तक सीमित करते हैं। परिणामस्वरूप, हम अंतर चिप संचार को कम करने और अंतिम स्तर कैश में हिट दर को बढ़ाने के लिए एक आभासी चिप के ऊपर गैर-समान कैश आर्किटेक्चर (एनयूसीए) योजना का लाभ उठाकर एक स्केलेबल फोटोनिक आधारित मल्टी-चिप वास्तुकला का प्रस्ताव करते हैं। उसके बाद हम सिलिकॉन नैनोकणों की मदद से जीपीयू के प्रदर्शन को बेहतर बनाने के लिए आगे बढ़ते हैं। हम जीपीयूएस के लिए एक ऊर्जा कुशल और स्केलेबल ऑप्टिकल इंटरकनेक्ट का प्रस्ताव देते हैं। हम समझदारी से घटकों को जीपीयू में विभिन्न प्रकार के समूहों में विभाजित करते हैं और इन समूहों को एक दूसरे के साथ वैकल्पिक रूप से संवाद करने में सक्षम बनाते हैं। नेटवर्क की देरी को कम करने के लिए, हम सुसंगतता और गैर-सुसंगत यातायात के लिए अलग-अलग नेटवर्क का उपयोग करते हैं। इसके अलावा, ऑप्टिकल इंटरकनेक्ट में स्थैतिक बिजली की खपत को कम करने के लिए, हम ऑन-चिप नेटवर्क ट्रैफ़िक की भविष्यवाणी के लिए एक उपन्यास जीपीयू विशिष्ट भविष्यवाणी योजना का प्रस्ताव करके ऑफ-चिप प्रकाश स्रोत को संशोधित करते हैं। अंत में, हम इस तथ्य को उजागर करते हैं कि जब तक सुरक्षा चिंताओं को संबोधित नहीं किया जाता है, तब तक तीसरे पक्ष के विक्रेताओं के लिए बड़े पैमाने पर ऑप्टिकल संचार समाधान

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