# CHARACTERIZATION AND MODELING OF ADVANCED CMOS DEVICES AT CRYOGENIC TEMPERATURES

SUMRETI GUPTA


DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY DELHI

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by

**SUMRETI GUPTA**

Department of Electrical Engineering

*Submitted*

*in fulfilment of the requirements of the degree of Doctor of Philosophy*

*to the*


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*Dedicated to*
*My Loving Family*

# Certificate

This is to certify that the thesis entitled "***Characterization and Modeling of Advanced CMOS Devices at Cryogenic Temperatures***", being submitted by Ms. **Sumreti Gupta** to the Indian Institute of Technology Delhi, is worthy of consideration for the award of the degree of **Doctor of Philosophy** in Department of Electrical Engineering and is a record of the original, bonafide research work carried out by her. The results contained in this thesis have not been submitted in part or in full, to any other University or Institute for the award of any degree or diploma.

I certify that she has pursued the prescribed course of research.

Date:

Place:

**Prof. Abhisek Dixit**
Professor,
Department of Electrical Engineering,
Indian Institute of Technology Delhi
Hauz Khas, New Delhi - 110016

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# *Abstract*

The present-day need to handle extremely complex computational problems efficiently and the promising results that quantum computers have demonstrated in this regard has catered attention of the researchers in the quantum computing domain. To achieve the targeted Noisy Intermediate Scale Quantum Computers (NISQ), researchers have been investigating the possible innovative solutions to address the current qubit scale-up challenge. The most promising solution that has emerged is the monolithic integration of qubits and control electronics in silicon, paving the path towards Quantum Integrated Circuits (QICs), which requires qubits and cryo-electronics to be operated at ∼1K to 4K temperature.

Research reports from the past have focused on the investigation and to some extent, modeling of planar bulk CMOS and 22nm FDSOI technology for cryogenic electronics applications. This thesis is targeted at cryogenic investigation of sub-10nm FinFETs and PDSOI devices, and the cryo-compatible industry standard compact models that comprehensively capture the low temperature physics using the most efficient semi-empirical equations. Detailed characterization and analysis of these advanced technology node devices has been done from 300K down to 10K temperature. The temperature trends for transfer and output characteristics; focusing on various electrical parameters such as threshold voltage, subthreshold swing and mobilities; are studied and the plausible underlying physical phenomena have been comprehended. Extensive experimental investigation of electron and hole mobilities in n- and p-channel FinFETs has been presented from 300K to 10K for variable geometry devices. It is found that short-channel FinFETs show mobility degradation that jeopardizes the cryogenic benefits. Further, multifrequency capacitance and conductance behavior of these devices has been evaluated to understand the effect of frequency coupled with cryo-temperatures on interface defects/traps, series resistance, dielectric response time and the tunneling currents.

After a detailed study on FinFETs, the impact of cryogenic temperature on the performance of SOI technology is evaluated. For SOI, self-heating due to the presence of thermally isolating BOX layer is a major concern. Thermal behavior of the 45nm PDSOI devices has been examined at cryogenic temperatures. Due to the reduced thermal conductivities at cryogenic temperatures, aggravated self-heating effect is

observed at low temperatures. Another major issue with PDSOI devices is the memory effect due to floating body charge instability, which has also been extensively addressed in this thesis.

The industry-standard compact models have been used over the years for commercial applications. With the advent of cryogenic applications of CMOS devices, these models need to be extended for these cryogenic effects. Hence, this thesis also presents a unified compact model that can be used to predict MOS device characteristics from room temperature down to cryogenic temperature by proposing modifications to BSIM-CMG and commercial PDKs. The circuit-level simulations are performed at cryogenic temperatures to understand the circuit implications of the low-temperature effects and to test the applicability of the proposed models.

# सार

वर्तमान समय में अत्यधिक जटिल कम्प्यूटेशनल समस्याओं को कुशलतापूर्वक संभालने की आवश्यकता है और इस संबंध में क्वांटम कंप्यूटरों ने जो आशाजनक परिणाम प्रदर्शित किए हैं, उन्होंने क्वांटम कंप्यूटिंग क्षेत्र में शोधकर्ताओं का ध्यान आकर्षित किया है। लक्षित नॉइज़ इंटरमीडिएट स्केल क्वांटम कंप्यूटर (एनआईएसक्यू) को प्राप्त करने के लिए, शोधकर्ताओं और उद्योगपतियों ने वर्तमान क्विबिट स्केल-अप चुनौती से निपटने के लिए संभावित नवीन समाधानों की जांच शुरू कर दी है। सबसे आशाजनक समाधान जो सामने आया है वह क्वांटम इंटीग्रेटेड सर्किट (क्यूआईसी) की दिशा में मार्ग प्रशस्त करने वाले सिलिकॉन में क्वैबिट और नियंत्रण इलेक्ट्रॉनिक्स का अखंड एकीकरण है, जिसके लिए ~१ कैल्विन से ४ कैल्विन पर संचालित होने के लिए क्वबिट और क्रायो-इलेक्ट्रॉनिक्स की आवश्यकता होती है।

अतीत की शोध रिपोर्टों ने मुख्य रूप से जांच और कुछ हद तक क्रायोजेनिक इलेक्ट्रॉनिक्स अनुप्रयोगों के लिए प्लेनर बल्क सीएमओएस और २२-एनएम एफडीएसओआई तकनीक के मॉडलिंग पर ध्यान केंद्रित किया है। यह थीसिस उप- १० -एनएम फिनफेट और पीडीएसओआई उपकरणों की क्रायोजेनिक जांच और क्रायो-संगत उद्योग मानक कॉम्पैक्ट मॉडल पर लक्षित है जो सबसे कुशल अर्ध-अनुभवजन्य समीकरणों का उपयोग करके कम तापमान भौतिकी को व्यापक रूप से कैप्चर करते हैं। इन उन्नत प्रौद्योगिकी नोड उपकरणों का विस्तृत लक्षण वर्णन और विश्लेषण ३०० कैल्विन से १० कैल्विन तक किया गया है। स्थानांतरण और आउटपुट विशेषताओं के लिए तापमान रुझान; थ्रेशोल्ड वोल्टेज, सबथ्रेशोल्ड स्विंग और मोबिलिटी जैसे विभिन्न विद्युत मापदंडों पर ध्यान केंद्रित करना; अध्ययन किया गया है और संभावित अंतर्निहित भौतिक घटनाओं को समझा गया है। विभिन्न ज्यामिति उपकरणों के लिए ३०० कैल्विन से १० कैल्विन तक एन- और पी-चैनल फिनफेट में इलेक्ट्रॉन और छेद मोबिलिटी की व्यापक प्रयोगात्मक जांच प्रस्तुत की गई है। यह पाया गया है कि शॉर्ट-चैनल फिनफेट मोबिलिटी में गिरावट दिखाते हैं जो क्रायोजेनिक लाभों को खतरे में डालता है। इसके अलावा, इंटरफ़ेस दोष/जाल, श्रृंखला प्रतिरोध, ढांकता हुआ प्रतिक्रिया समय और सुरंग धाराओं पर क्रायो-तापमान के साथ युग्मित आवृत्ति के प्रभाव को समझने के लिए इन उपकरणों की बहुआवृत्ति समाई और चालन व्यवहार का मूल्यांकन किया गया है।

फिनफेट पर एक विस्तृत अध्ययन के बाद, एसओआई प्रौद्योगिकी के प्रदर्शन पर क्रायोजेनिक तापमान के प्रभाव का मूल्यांकन किया गया है। एसओआई के लिए, थर्मल इंसुलेटिंग बॉक्स परत की उपस्थिति के कारण स्व-हीटिंग एक प्रमुख चिंता का विषय है। क्रायोजेनिक तापमान पर ४५ एनएम पीडीएसओआई उपकरणों के थर्मल व्यवहार की जांच की गई है। क्रायोजेनिक तापमान पर तापीय चालकता कम होने के कारण, कम तापमान पर एकत्रित स्व-ताप प्रभाव देखा जाता है। पीडीएसओआई उपकरणों के साथ एक और प्रमुख मुद्दा फ्लोटिंग बॉडी चार्ज अस्थिरता के कारण मेमोरी प्रभाव है, जिसे इस थीसिस में भी बड़े पैमाने पर संबोधित किया गया है।

उद्योग-मानक कॉम्पैक्ट मॉडल का उपयोग वर्षों से व्यावसायिक अनुप्रयोगों के लिए किया जाता रहा है और सीएमओएस उपकरणों के क्रायोजेनिक अनुप्रयोगों के आगमन के साथ, इन मॉडलों को उपरोक्त क्रायोजेनिक प्रभावों के लिए परिष्कृत करने की आवश्यकता है। इसलिए, यह थीसिस एक एकीकृत कॉम्पैक्ट मॉडल भी प्रस्तुत करती है जिसका उपयोग बीएसआईएम-सीएमजी और वाणिज्यिक पीडीके में संशोधन का प्रस्ताव करके कमरे के तापमान से क्रायोजेनिक तापमान तक एमओएस उपकरणों की विशेषताओं की भविष्यवाणी करने के लिए किया जा सकता है। कम तापमान प्रभावों के सर्किट निहितार्थ को समझने और प्रस्तावित मॉडल की प्रयोज्यता का परीक्षण करने के लिए सर्किट-स्तरीय सिमुलेशन क्रायोजेनिक तापमान पर किया जाता है। कुल मिलाकर, यह थीसिस संभावित उन्नत प्रौद्योगिकी नोड उपकरणों के क्रायोजेनिक व्यवहार के बारे में प्रारंभिक ज्ञान प्रदान करती है जो भविष्य के क्वांटम कंप्यूटिंग उद्योग को चला सकते हैं।

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# Physical Constants

| Name | Symbol | Value |
|---|---|---|
| Dielectric constant of Silicon | $\epsilon_{\mathrm{Si}}$ | 11.7 |
| Dielectric constant of Silicon dioxide | $\epsilon_{\mathrm{SiO_2}}$ | 3.9 |
| Dielectric constant of Hafnium oxide | $\epsilon_{\mathrm{HFO_2}}$ | 20 |
| Bandgap of Silicon | $E_{\mathrm{g}}$ | 1.12 eV |

# Symbols

| Symbol | Description |
|---|---|
| $N_{fin}$ | No. of fins |
| $H_{fin}$ | Fin Height |
| $W_{tot}$ | Total Width |
| $L_g$ | Designed gate length |
| $V_{gs}$ | Gate-to-source voltage |
| $V_{ds}$ | Drain-to-source voltage |
| $\mu_{eff}$ | Effective mobility |
| $V_t$ | Threshold voltage |
| $V_{th}$ | Thermal voltage |
| $L_{eff}$ | Effective length |
| $Q_i$ | Inversion charge |
| $C_{ox}$ | Oxide capacitance |
| $t_{inv}$ | Inversion thickness |
| $C_{inv}$ | Inversion capacitance |
| $g_m$ | Transconductance |
| $g_{ds}$ | Output conductance |
| $\Delta L$ | Channel length reduction factor |
| $R_{ch}$ | Channel resistance |
| $V_{od}$ | Overdrive voltage |
| $R_S$ | Series resistance |
| $V_{fb}$ | Flatband voltage |
| $\beta_{acc}$ | Accumulation region surface potential quotient |
| $\tau_{sub}$ | Substrate time constant |
| $R_{th}$ | Thermal resistance |

| | |
|---|---|
| $K_{th}$ | Thermal conductance |
| $T_{chuck}$ | Chuck temperature |
| $\Delta T$ | Temperature rise |
| $q_b$ | Body charge |
| $TD_f$ | Output fall-time delay |
| $I_{on}$ | On current |
| $t$ | Time |
| $T$ | Temperature |

# Abbreviations

| Abbreviation | Description |
|---|---|
| **BEOL** | **B**ack **E**nd **O**f **L**ine |
| **BSIM** | **B**erkeley **S**hort-**C**hannel **IGFET** Model |
| **BTI** | **B**ias **T**emperature **I**nstability |
| **CCR** | **C**losed **C**ycle **R**efrigerator |
| **CMG** | **C**ommon **M**ulti-**G**ate |
| **CMOS** | **C**omplementary **M**etal **O**xide **S**emiconductor |
| **CV** | **C**apacitance versus **V**oltage |
| **DIBL** | **D**rain **I**nduced **B**arrier **L**owering |
| **DR** | **D**ilution **R**efrigerator |
| **DUT** | **D**evice **U**nder **T**est |
| **EOT** | **E**quivalent **O**xide **T**hickness |
| **FinFET** | **F**in **F**ield **E**ffect **T**ransistor |
| **GSWU** | **G**uard **S**witch **U**nit |
| **HCD** | **H**ot **C**arrier **D**egradation |
| **IC** | **I**ntegrated **C**ircuit |
| **ITRS** | **I**nternational **T**echnology **R**oadmap for **S**emiconductors |
| **MFCMU** | **M**ulti **F**requency **C**apacitance **M**easurement **U**nit |
| **MOSFET** | **M**etal **O**xide **S**emiconductor **F**ield **E**ffect **T**ransistor |
| **NISQ** | **N**oisy **I**ntermediate **S**cale **Q**uantum |
| **PDK** | **P**rocess **D**esign **K**it |
| **QC** | **Q**uantum **C**omputer |
| **QD** | **Q**uantum **D**ot |
| **QIC** | **Q**uantum **I**ntegrated **C**ircuit |
| **qLPDC** | **Q**uantum **L**ow-**D**ensity **P**arity **C**heck |
| **QPU** | **Q**uantum **P**rocessing **U**nit |

| | |
|---|---|
| **RSU** | **R**emote **S**witch **U**nit |
| **RTS** | **R**andom **T**elegraph **S**ignal |
| **SCE** | **S**hort **C**hannel **E**ffects |
| **SCUU** | **S**MU **C**MU **U**nify **U**nit |
| **SHE** | **S**elf **H**eating **E**ffect |
| **SHF** | **S**elf **H**eating **F**ree |
| **SOC** | **S**ystem **O**n **C**hip |
| **SOI** | **S**ilicon **O**n **I**nsulator |
| **SS** | **S**ubthreshold **S**wing |
| **TCAD** | **T**echnology **C**omputer **A**ided **D**esign |
| **TDDB** | **T**ime **D**ependent **D**ielectric **B**reakdown |
| **TEM** | **T**ransmission **E**lectron **M**icroscopy |
| **TMP** | **T**urbo **M**olecular **P**ump |
| **TPS** | **T**urbo **P**umping **S**ystem |
| **VCO** | **V**oltage **C**ontrolled **O**scillator |
| **WGFMU** | **W**aveform **G**enerator **F**ast **M**easurement **U**nit |