EFFECTS OF INTERFACE STATES ON CHARGE TRANSFER IN CHARGE - COUPLED DEVICES

By

SUDHIR KUMAR MADAN

Department of Electrical Engineering

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CERTIFICATE

This is to certify that the thesis entitled ' Effects of Interface States on Charge Transfer in Charge-Coupled Devices' being submitted by Sudhir Kumar Madan to the Department of Electrical Engineering, Indian Institute of Technology, Delhi, for the award of degree of Doctor of Philosophy is a record of bonafide research work carried out by him under my supervision and guidance and in my opinion it has reached the standard fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted to any other Institution for the award of any Degree or Diploma.

B. Bhaumik
Department of Electrical Engineering
Indian Institute of Technology, Delhi

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ABSTRACT

From the very beginning, interface states have been identified as one of the major source of performance limitations of charge-coupled devices (CCDs). Various performance limitations due to these states have been further investigated in this thesis and the interaction of the signal charge with these states has been studied in detail.

A new type of signal degradation, namely the feed forward of charge in CCDs has been theoretically as well as experimentally established in this thesis. Feed forward arises because of the modulation of the electric field due to the signal charge and the presence of interface states. Feed forward manifests itself at the output in the form of a pulse coming out earlier than the main signal pulse and it modifies the transfer function.

Explicit expressions for the feed forward of charge have been obtained for various clocking schemes. Experiments as well as the analysis show that the interelectrode gap plays an important role in determining the feed forward and the gap would tend to reduce the effect. Computer calculations have also been done to quantify the feed forward effect. Various experiments performed show a good agreement between the experimental data and the theoretical models.

The analysis done for feed forward was extended to study the effect of barrier shape on CTI for the push clock operation.

A number of hitherto unknown features of charge movement have been pointed out. Based on the above analysis, a new stepped push clock was used to obtain lower values of CTI.

It has been experimentally shown that the model based on interface-state effects only, fails to explain the data on some of the devices. The existence of surface potential fluctuations as a possible reason for its failure has been investigated. A model has also been developed for this purpose and it has been shown that these fluctuations would slow down the charge transfer process. Since the existing theories on charge transfer have overlooked the effect of these fluctuations, a second look may be required.

A number of new clocking schemes aimed at reducing the CTI due to the interface states have been explored by suitably shaping the clocking waveforms so that the edge areas wetted by both the ONE and FATZERO (FZ) charges become equal. Theoretically it has been shown that one of these clocking schemes has great potential to reduce the CTI in surface-channel CCDs to a level which is normally obtained only with buried-channel devices.

In the thesis, a novel technique has been demonstrated to measure the interface state density using CCDs. The new technique has been compared with other CCD-based techniques and it has been shown that the new technique offers an advantage of measuring the interface state density near the band edge by operating the CCD at any convenient low frequency. This is not possible with any other technique where the CCD would have to be clocked at high frequencies to measure the interface state density near the band edge. In most of the cases it should also be possible to scan a wider energy range with the new technique.

Experimental observation of avalanche multiplication in charge-coupled devices has been made during the course of this work, we believe for the first time. Various simple experiments have been performed to characterize it. Experimental observations show that the avalanche multiplication takes place when the electrons are made to fall down a steep barrier(similar to that in 2-phase CCDs) of more than 8 V. A simple model has been developed which explains the experimental results reasonably well. Since the avalanche multiplication is likely to occur at a much lower voltage than the oxide breakdown voltage, it would impose the upper limit on the maximum clock amplitude. Hence it would determine the minimum obtainable value of CTI due to the interface states (edge effect).

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