

IDENTIFICATION & LOCATION OF FAULTS IN DC MICROGRIDS

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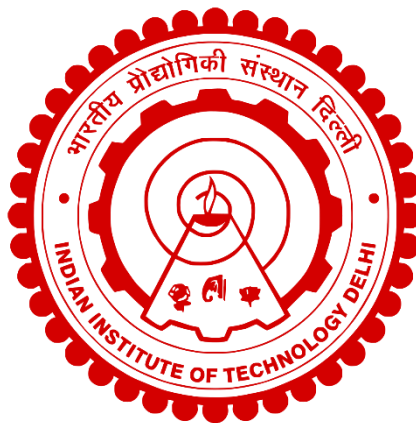
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to the



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Dedicated to my mother ...

Certificate

This is to certify that the dissertation entitled '**Identification & Location of Faults in DC Microgrids**', being submitted by **Mr. Vaibhav Nougain** for the award of the degree of **Doctor of Philosophy** is a record of bonafide research work carried out by him in the Department of Electrical Engineering at Indian Institute of Technology Delhi, New Delhi.

Mr. Vaibhav Nougain has worked under my supervision and has fulfilled the requirements for the submission of this dissertation, which to my knowledge has reached the requisite standard. The results obtained here have not been submitted to any other University or Institute for the award of any degree.

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Abstract

The focus of the thesis is to first identify the fault and then locate its position in DC distribution systems also known as DC microgrids. DC systems have a lower impedance to offer for a fault in comparison to their AC counterpart which results in high di/dt and high steady-state current. This causes the requirement of fast fault isolation which has been suggested to be within 5ms of fault inception. Since di/dt is very high upon fault inception, current limiting reactors (CLRs) can be used externally to limit the rate of increase of current. If used, CLR also serves as a local differentiator for fast, robust, and selective protection. Low voltage and medium voltage DC systems have short lines or cable lengths (<10km) for power distribution. DC fault transients have natural frequency of oscillation, $f_n < 500\text{Hz}$. Based on the wavelength of propagation, $\lambda f = v$, lumped R-L parameters can be used in the analysis. Different attributes like security, dependability, selectivity, sensitivity to high resistance faults, fault detection time, computational burden, degree of external modification, robustness to white Gaussian noise in measurement, etc are used to validate different proposed fault identification and location schemes for DC systems.

Fault Identification: A high rate of rising of current due to discharging converter capacitor can damage the interfacing converter switches in case of improper control logic. Even if the control is proper, the converter control is bypassed to limit the current affecting the power transfer in the system. Either way, there is an indispensable requirement for a fault identification scheme that can detect a fault and identify the faulty section in the system. This allows the operation of solid-state circuit breakers (SSBCs) and isolators to isolate the faulty line/cable in the microgrid.

- To address the issue of fault identification for DC microgrids without any external modification, a localized backup fault identification scheme is proposed. The scheme uses running autoregressive smoothing average of local current and voltage signals to identify the fault on the DC side up to 5Ω . Additionally, adaptive thresholds are derived for the wider application of the scheme. The proposed method is simple and does not require any external modifications like current limiting reactors. As a trade-off, the application of the method is limited to low resistance faults. Also, the method has selectivity issues where internal and forward external faults may not be differentiated between one another.
- Focussing on the shortcomings of previous work, the proposed work is aimed to improve the application of fault identification methods for low as well as high resistance faults. The method has good selectivity which means it is easily able to differentiate between internal and forward external DC faults. The algorithm detects faults with fault resistance as high as 200Ω . The method also introduces the concept of cyber resiliency of a protection scheme. The proposed fault identification scheme is validated to be robust against cyber attacks in the system. The analysis involves using current limiting reactors (CLR) as external modifications in the medium voltage microgrids. Using CLR in the system limits the rate of increase of fault current.

Fault Location: Once the faulty section is identified, location methods can accurately calculate the distance of the fault in the identified faulty segment. Locating the fault point accurately helps in clearing the fault in time, acting as the key to the rapid restoration of faulty distribution lines and cables.

- A single-terminal fault location method is proposed that is robust to variations of key parameters (e.g. sampling frequency, system parameters, etc.) and performs particularly well for low resistance faults in low voltage DC systems. The proposed method uses local measurements to estimate the current experienced by the other terminals affected by the contingency. This mimics the strategy followed by double terminal methods

that require communications and decouples the accuracy of the methodology from the fault resistance. The algorithm is based on an iterative approach that starts from an initial guess of the fault location. This is used to achieve faster convergence and better accuracy than other approaches in founding the literature. The method is however limited to low fault resistances up to 5Ω only.

- A double-terminal fault location method is proposed focussing on the shortcomings of the previous single-terminal fault location method. The proposed work is aimed to improve the application of fault location methods for low as well as high resistance faults. The algorithm accurately locates faults with fault resistance as high as 200Ω . Based on the availability of communication and sensors, different terminals can be used to increase the reliability of the proposed fault location method.

सारांश

थीसिस का फोकस पहले दोष की पहचान करना है और फिर DC वितरण प्रणाली में इसकी स्थिति का पता लगाना है जिसे DC माइक्रोग्रिड भी कहा जाता है। DC सिस्टम में उनके एसी समकक्ष की तुलना में एक गलती की पेशकश करने के लिए कम प्रतिबाधा होती है जिसके परिणामस्वरूप उच्च di/dt और उच्च स्थिर-अवस्था करंट होता है। यह तेजी से गलती अलगाव की आवश्यकता का कारण बनता है जो कि गलती की स्थापना के 5ms के भीतर होने का सुझाव दिया गया है। चूंकि di/dt दोष प्रारंभ होने पर बहुत अधिक है, वर्तमान सीमित रिएक्टरों (सीएलआर) को वर्तमान की वृद्धि की दर को सीमित करने के लिए बाहरी रूप से उपयोग किया जा सकता है। यदि उपयोग किया जाता है, तो सीएलआर तेज, मजबूत और चयनात्मक सुरक्षा के लिए स्थानीय विभेदक के रूप में भी कार्य करता है। कम वोल्टेज और मध्यम वोल्टेज डीसी सिस्टम में बिजली वितरण के लिए छोटी लाइनें या केबल की लंबाई (<10km) होती है।

DC गलती यात्रियों में स्वाभाविक है दोलन की आवृत्ति, $f_n < 500\text{Hz}$. प्रसार की तरंग दैर्ध्य के आधार पर, $\lambda f = v$, गांठ वाले आर-एल पैरामीटर विश्लेषण में उपयोग किया जा सकता है। विभिन्न विशेषताओं जैसे सुरक्षा, निर्भरता, चयनात्मकता, उच्च प्रतिरोध दोषों के प्रति संवेदनशीलता, दोष का पता लगाने का समय, कम्प्यूटेशनल बोझ, बाहरी संशोधन की डिग्री, माप में सफेद गॉसियन शोर की मजबूती, आदि का उपयोग डीसी सिस्टम के लिए विभिन्न प्रस्तावित दोष पहचान और स्थान योजनाओं को मान्य करने के लिए किया जाता है। .

गलती की पहचान: निर्वहन के कारण करंट बढ़ने की उच्च दर कनवर्टर कैपेसिटर अनुचित नियंत्रण तर्क के मामले में इंटरफेसिंग कनवर्टर स्विच को नुकसान पहुंचा सकता है। यहां तक कि अगर नियंत्रण उचित है, तो बिजली हस्तांतरण को प्रभावित करने वाले वर्तमान को सीमित करने के लिए कनवर्टर नियंत्रण को बायपास किया जाता है प्रणाली। किसी भी तरह से, एक गलती पहचान योजना के लिए एक अनिवार्य आवश्यकता है जो एक गलती का पता लगा सकती है और सिस्टम में दोषपूर्ण खंड की पहचान कर सकती है। यह माइक्रोग्रिड में दोषपूर्ण लाइन/केबल को अलग करने के लिए

सॉलिड-स्टेट सर्किट ब्रेकर (एसएसबीसी) और आइसोलेटर्स के संचालन की अनुमति देता है।

- बिना किसी बाहरी संशोधन के DC माइक्रोग्रिड्स के लिए दोष पहचान के मुद्दे को हल करने के लिए, एक स्थानीयकृत बैकअप दोष पहचान योजना प्रस्तावित है। यह योजना डीसी की ओर 5Ω तक की खराबी की पहचान करने के लिए स्थानीय करंट और वोल्टेज सिग्नलों के रनिंग ऑटोरेग्रेसिव स्मूथिंग औसत का उपयोग करती है। इसके अतिरिक्त, योजना के व्यापक अनुप्रयोग के लिए अनुकूली सीमाएँ प्राप्त की जाती हैं। प्रस्तावित विधि सरल है और इसमें वर्तमान सीमित रिएक्टरों जैसे किसी बाहरी संशोधन की आवश्यकता नहीं है। ट्रेड-ऑफ के रूप में, विधि का अनुप्रयोग कम प्रतिरोध दोषों तक सीमित है। इसके अलावा, विधि में चयनात्मकता के मुद्दे हैं जहां आंतरिक और आगे के बाहरी दोषों को एक दूसरे के बीच अंतर नहीं किया जा सकता है।
- पिछले कार्य की कमियों पर ध्यान केंद्रित करते हुए, प्रस्तावित कार्य का उद्देश्य कम और साथ ही उच्च प्रतिरोध दोषों के लिए दोष पहचान विधियों के अनुप्रयोग में सुधार करना है। विधि में अच्छी चयनात्मकता है जिसका अर्थ है कि यह आसानी से आंतरिक और आगे बाहरी डीसी दोषों के बीच अंतर करने में सक्षम है। एल्गोरिद्म 200Ω तक के फॉल्ट प्रतिरोध वाले फॉल्ट का पता लगाता है। विधि एक सुरक्षा योजना के साइबर लचीलेपन की अवधारणा को भी प्रस्तुत करती है। सिस्टम में साइबर हमलों के खिलाफ प्रस्तावित दोष पहचान योजना को मजबूत होने के लिए मान्य किया गया है। विश्लेषण में मध्यम वोल्टेज माइक्रोग्रिड्स में बाहरी संशोधनों के रूप में वर्तमान सीमित रिएक्टरों (सीएलआर) का उपयोग करना शामिल है। सिस्टम में सीएलआर का उपयोग फॉल्ट करंट के बढ़ने की दर को सीमित करता है।

एक बार दोषपूर्ण खंड की पहचान हो जाने के बाद, स्थान विधियाँ पहचाने गए दोषपूर्ण खंड में दोष की दूरी की सही गणना कर सकती हैं। फॉल्ट प्वाइंट का सटीक पता लगाने

से समय पर फॉल्ट को साफ करने में मदद मिलती है, जो दोषपूर्ण वितरण लाइनों और केबलों की तेजी से बहाली की कुंजी के रूप में कार्य करता है।

- एक सिंगल-टर्मिनल फॉल्ट लोकेशन मेथड प्रस्तावित है जो प्रमुख मापदंडों (जैसे नमूना आवृत्ति, सिस्टम पैरामीटर, आदि) की विविधताओं के लिए मजबूत है और कम वोल्टेज डीसी सिस्टम में कम प्रतिरोध दोषों के लिए विशेष रूप से अच्छा प्रदर्शन करता है। प्रस्तावित विधि आकस्मिकता से प्रभावित अन्य टर्मिनलों द्वारा अनुभव किए गए वर्तमान का अनुमान लगाने के लिए स्थानीय माप का उपयोग करती है। यह डबल टर्मिनल विधियों के बाद की रणनीति की नकल करता है जिसके लिए संचार की आवश्यकता होती है और दोष प्रतिरोध से कार्यप्रणाली की सटीकता को कम करता है। एल्गोरिथ्म पुनरावृत्त दृष्टिकोण पर आधारित है जो गलती स्थान के प्रारंभिक अनुमान से शुरू होता है। इसका उपयोग साहित्य की स्थापना में अन्य दृष्टिकोणों की तुलना में तेजी से अभिसरण और बेहतर सटीकता प्राप्त करने के लिए किया जाता है। हालांकि विधि केवल 5Ω तक कम दोष प्रतिरोधों तक सीमित है।
- पिछले सिंगल-टर्मिनल फॉल्ट लोकेशन मेथड की कमियों पर ध्यान केंद्रित करते हुए एक डबल-टर्मिनल फॉल्ट लोकेशन मेथड प्रस्तावित है। प्रस्तावित कार्य का उद्देश्य कम और उच्च प्रतिरोध दोषों के लिए गलती स्थान विधियों के अनुप्रयोग में सुधार करना है। एल्गोरिथ्म 200Ω तक के फॉल्ट प्रतिरोध वाले फॉल्ट का सटीकता से पता लगाता है। संचार और सेंसर की उपलब्धता के आधार पर, प्रस्तावित गलती स्थान पद्धति की विश्वसनीयता बढ़ाने के लिए विभिन्न टर्मिनलों का उपयोग किया जा सकता है।

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Abbreviations

CLR	Current Limiting Reactor
CPL	Constant Power Loads
DCR	Differential Current Relay
DERs	Distributed Energy Resources
DWT	Discrete Wavelet Transform
DoS	Denial of Service
ECIs	External Cyber Intrusion
ESS	Energy Storage Systems
FDTL	Frequency-dependent Transmission Model
FFT	Fast Fourier Transform
HRFs	High Resistance Faults
IEDs	Intelligent Electronic Devices
LAN	Local Area Network
LV, MV DC	Low Voltage, Medium Voltage Direct Current
N-PTG	Negative Pole to Ground
OHL	Overhead Line
POC	Passive Oscillator Circuit
PPU	Probe Power Unit
PTP	Pole to Pole
P-PTG	Positive Pole to Ground
PV	Photovoltaics
ROTV	Ratio of Transient Voltages
RASA	Running Autoregressive Smoothing Average
SSCBs	Solid State Circuit Breakers
SMGs	Sub-microgrids
SoC	State of Charge

TSA	Time Synchronization Attack
UGC	Underground Cable
WGN	White Gaussian Noise