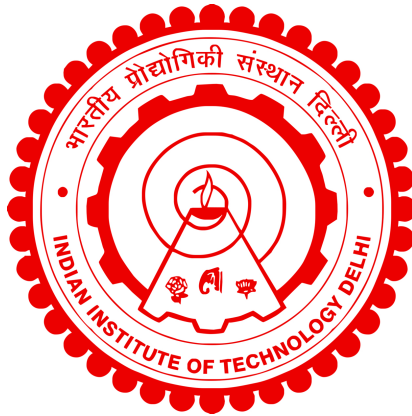


CHARACTERIZATION AND MODELING OF FINFETS AT CRYOGENIC TEMPERATURES FOR SCALABLE SEMICONDUCTING QUBITS

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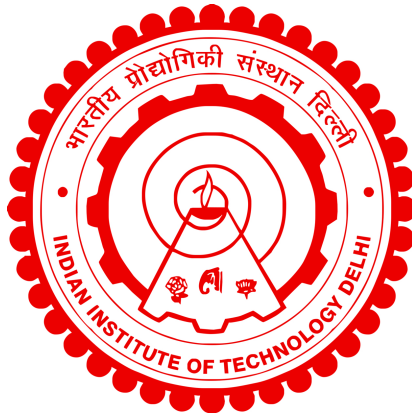
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Submitted

in fulfillment of the degree of Doctor of Philosophy

to the



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*Dedicated to
my family and teachers who have consistently motivated
me to engage in the noble pursuit of science, as well as to
those who aspire to challenge the limits of quantum
computing with resolute resolve and curiosity.*

Certificate

This is to certify that the thesis entitled “**Characterization and Modeling of FinFETs at Cryogenic Temperatures for Scalable Semiconducting Qubits**”, submitted by **Sujit Kumar Singh** to the Indian Institute of Technology Delhi, for the award of the degree of **Doctor of Philosophy** in Electrical Engineering, is a record of the original, bonafide research work carried out by him under our supervision and guidance. The thesis has reached the standards fulfilling the requirements of the regulations related to the award of the degree.

The results contained in this thesis have not been submitted in part or in full to any other University or Institute for the award of any degree or diploma to the best of our knowledge.



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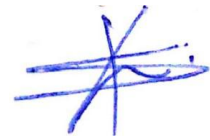
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Abstract

In the current era of Noisy Intermediate-Scale Quantum (NISQ) based quantum computers, as many as 1121 qubits can be integrated into a single Quantum Processing Unit (QPU). However, for these quantum computers to be used as general-purpose computers solving complex problems, the number of qubits in a QPU must be in millions. To achieve this milestone, the use of industrial CMOS platforms is increasingly being proposed as a feasible alternative. The industrial CMOS platforms offer tight packaging densities, small on-wafer footprints and excellent control over the geometry of the fabricated devices, which can, in principle, allow large-scale integration of thousands of qubits into a small QPU volume. However, as the physics behind the operation of quantum devices in QPU differs drastically from the operation of classical FETs, the design of quantum devices in the industrial CMOS platform has been extremely challenging.

To help circumvent this problem, the presented thesis showcases how an industrial short channel FinFET, designed in 10-12 nm technology node can be used to realize quantum devices of a QPU such as Single Electron Transistors (SETs), Quantum Dot Thermometers (QDT), Coulomb Blockade Thermometers (CBTs) operational at cryogenic temperatures. Results show that the cryogenic operation of these industry standard short channel FinFETs operating at its subthreshold bias regime leads to the formation of a gate-defined Quantum Dot (QD) in the channel, which is electrostatically confined by the potential barriers in the Lightly Doped (LDD) region of the channel just below the gate spacers. The small channel volume of these FETs allows the channel's QD to have extremely small spherical equivalent diameters (10 to 15 nm). This allows these devices to work in QD / Quantum mode for temperatures as high as 40 K, where only a handful of quantum devices have been reported to be operational. The quantum mode of operation in these devices thus allows them to be used as a CMOS-friendly alternative to traditional non-CMOS processing-based large-footprint devices such as SETs, QDTs, CBTs, and qubits commonly used in a QPU.

The performance of these industrial FinFETs operating at 8 K is comparable to the state-of-the-art quantum devices operated at much smaller cryogenic temperatures (10 mK). Moreover, as these proposed FinFET based QD devices can be operated at relatively higher cryogenic temperature stages (above 7.8 K) where the thermal

cooling capacity of the cryogenic hardware is sufficiently large, a large scale QPU volume can be realised/tolerated within the thermal budget of the cryogenic cooling assembly.

Although the QD-based operation in the cryogenic FinFETs is distinctive for a small gate bias range, experimental results show that the variation in the Number of Fins and/or Threshold voltage enables the precise tuning of the gate bias range in which the QD-based operation is desired to be operated. The impact of other geometry-dependent parameters, such as the Number of Fingers, masked gate length, and channel type (p-type and n-type) on the properties of the channel's QD is explored in grave detail. This geometry-dependent study is expected to serve as a rule book for any CMOS device engineer to help build QD-based devices using these FinFETs. The QD size is also found to be highly uniform across identical geometries of FinFETs, which helps further advocate the precise control of the QD properties offered by these industrial CMOS platforms.

To help feasibly design and validate the operation of these FinFET based QD devices before its physical fabrication, a Verilog-A based compact model is proposed. The proposed model is built on top of the BSIM-CMG compact model and accurately captures the classical performance and quantum performance of these FinFETs across the wide dynamic temperature range of 300 K down to 8 K. The proposed model can be used to design the cryogenic-CMOS-based control and readout electronics of a co-integrated QPUs. The model helps evaluate the performance of Hybrid SET-FET circuits built entirely using the proposed FinFETs. The challenges with such full-CMOS-based design of hybrid circuits and their solutions are discussed in grave detail to fully comprehend the design prospects with these new FinFET-based QD technologies.

COMSOL multiphysics simulations of the QD performance in FinFETs operating at cryogenic temperatures are also presented in this work to showcase how the body bias can be used to fine-tune the charge sensitivity of the QD formed in the channel. A compact modeling framework for the simulation of a silicon spin qubit is also presented to help simulate simple quantum-gated operations in popular stimulative platforms such as MATLAB.

सार

वर्तमान युग में शोरयुक्त मध्यम-स्केल क्वांटम कंप्यूटरों के विकास के साथ, एकल क्वांटम प्रोसेसिंग यूनिट (क्यूपीयू) में 1121 क्यूबिट्स को एकीकृत किया जा सकता है। हालाँकि, इन क्वांटम कंप्यूटरों का उपयोग सामान्य-उद्देश्य कंप्यूटर के रूप में जटिल समस्याओं को हल करने के लिए करने के लिए, क्यूपीयू में क्यूबिट्स की संख्या लाखों में होनी चाहिए। इस मुकाम को हासिल करने के लिए, औद्योगिक धातु-ऑक्साइड-सेमीकंडक्टर (सीएमओएस) का उपयोग एक व्यवहार्य विकल्प के रूप में तेजी से प्रस्तावित किया जा रहा है। औद्योगिक सीएमओएस उच्च पैकेजिंग घनत्व, छोटे ऑन-वेफर फुटप्रिंट और निर्मित उपकरणों के ज्यामिति पर उत्कृष्ट नियंत्रण प्रदान करते हैं, जो सिद्धांत रूप से हजारों क्यूबिट्स को एक छोटे क्यूपीयू वॉल्यूम में बड़े पैमाने पर एकीकृत करने की अनुमति दे सकते हैं। हालाँकि, क्यूपीयू में क्वांटम उपकरणों के संचालन के पीछे का भौतिकी क्लासिकल फील्ड इफेक्ट ट्रांजिस्टर (एफईटी) के संचालन से काफी भिन्न है, इसलिए औद्योगिक सीएमओएस में क्वांटम उपकरणों के डिजाइन में अत्यधिक चुनौतियाँ आई हैं। इस समस्या को हल करने के लिए, प्रस्तुत प्रबंध दिखाता है कि कैसे 10-12 नैनोमीटर तकनीकी नोड में डिजाइन किए गए औद्योगिक शॉर्ट चैनल फिनफेट का उपयोग क्यूपीयू के क्वांटम उपकरणों जैसे सिंगल इलेक्ट्रॉन ट्रांजिस्टर (एसईटी), क्वांटम डॉट थर्मामीटर (क्यूडीटी), और कूलंब ब्लॉकडे थर्मामीटर (सीबीटी) को क्रायोजेनिक तापमान पर वास्तविकता में लाने के लिए किया जा सकता है। परिणाम दर्शाते हैं कि इन उद्योग मानक शॉर्ट चैनल फिनफेट का क्रायोजेनिक संचालन उनके सबथ्रेशोल्ड बायस क्षेत्र में गेट-परिभाषित क्वांटम डॉट (क्यूडी) के निर्माण की ओर ले जाता है, जिसे चैनल के हल्के डोप किए गए ड्रेन (एलडीडी) क्षेत्र में पोटेंशियल बाधाओं द्वारा इलेक्ट्रोस्टैटिक रूप से संलग्न किया गया है, जो गेट स्पेसर के ठीक नीचे होता है। इन एफईटी के छोटे चैनल वॉल्यूम के कारण चैनल का क्यूडी अत्यंत छोटे गोलाकार समकक्ष व्यास (10 से 15 नैनोमीटर) रखने में सक्षम होता है। यह इन उपकरणों को 40 केल्विन तक के तापमान पर क्यूडी / क्वांटम मोड में कार्य करने की अनुमति देता है, जहाँ केवल कुछ क्वांटम उपकरणों की रिपोर्ट की गई है कि वे कार्यशील हैं। इन उपकरणों में क्वांटम मोड का संचालन उन्हें क्यूपीयू में सामान्यतः उपयोग होने वाले पुराने नॉन-सीएमओएस प्रोसेसिंग-आधारित बड़े-फुटप्रिंट उपकरणों जैसे एफईटी, क्यूडीटी, सीबीटी और क्यूबिट्स के मुकाबले सीएमओएस-अनुकूल विकल्प के रूप में उपयोग करने की अनुमति देता है। 8 केल्विन पर काम करने वाले इन औद्योगिक फिनफेट का प्रदर्शन अत्यधिक छोटे क्रायोजेनिक तापमान (10 मिली केल्विन) पर काम करने वाले प्रचालित क्वांटम उपकरणों के साथ तुलनीय है। इसके अलावा, चूंकि प्रस्तावित फिनफेट आधारित क्यूडी उपकरणों को अपेक्षाकृत उच्च क्रायोजेनिक तापमान स्तरों (7.8 केल्विन से अधिक) पर संचालित किया जा सकता है जहाँ क्रायोजेनिक हार्डवेयर की ठंडा करने की क्षमता काफी बड़ी होती है, एक बड़े पैमाने पर क्यूपीयू वॉल्यूम को क्रायोजेनिक कूलिंग असेंबली के थर्मल बजट के भीतर वास्तविकता में लाया जा सकता है। हालांकि, क्रायोजेनिक फिनफेट में क्यूडी-आधारित संचालन एक छोटे गेट बायस सीमा के लिए विशिष्ट है, प्रयोगात्मक परिणाम दिखाते हैं कि फिन की संख्या और/या थ्रेशोल्ड वोल्टेज में भिन्नता क्यूडी-आधारित संचालन को जिस गेट बायस सीमा में संचालित किया जाना है, उसे सटीक रूप से निर्धारित करने में सक्षम बनाती है। अन्य ज्यामिति-निर्भर

पैरामीटर जैसे फिंगर्स की संख्या, मास्क गेट लंबाई, और चैनल प्रकार (पी-प्रकार और एन-प्रकार) के चैनल के क्यूडी की गुणधर्मों पर प्रभाव का विस्तार से अध्ययन किया गया है। यह ज्यामिति-निर्भर अध्ययन किसी भी सीएमओएस डिवाइस इंजीनियर के लिए इस फिनफेट का उपयोग करके क्यूडी-आधारित उपकरण बनाने में मदद करने के लिए एक नियम पुस्तक के रूप में कार्य करने की अपेक्षा की जाती है। क्यूडी का आकार भी समान फिनफेट ज्यामितियों के बीच अत्यधिक समान पाया गया है, जो इन औद्योगिक सी-एमओएस द्वारा प्रदान की गई क्यूडी गुणधर्मों के सटीक नियंत्रण को और अधिक समर्थन देता है। इन फिनफेट आधारित क्यूडी उपकरणों के संचालन को भौतिक निर्माण से पहले व्यावहारिक रूप से डिजाइन और मान्य करने में मदद करने के लिए, एक वेरिलोग-ए आधारित कॉम्पैक्ट मॉडल प्रस्तावित किया गया है। प्रस्तावित मॉडल बीएसआईएम-सीएमजी कॉम्पैक्ट मॉडल के शीर्ष पर बनाया गया है और 300 केल्विन से 8 केल्विन के विस्तृत तापमान श्रृंखला में इन फिनफेट के क्लासिकल और क्वांटम प्रदर्शन को सटीक रूप से दर्शाने करता है। प्रस्तावित मॉडल का उपयोग सह-इंटीग्रेटेड क्यूपीयू के क्रायोजेनिक-सीएमओएस आधारित नियंत्रण और रीडआउट इलेक्ट्रॉनिक्स के डिजाइन में किया जा सकता है। यह मॉडल प्रस्तावित फिनफेट का उपयोग करके पूरी तरह से निर्मित हाइब्रिड एसईटी-एफईटी सर्किट के प्रदर्शन का मूल्यांकन करने में मदद करता है। हाइब्रिड सर्किट के पूर्ण-सीएमओएस-आधारित डिजाइन के साथ चुनौतियों और उनके समाधानों पर विस्तार से चर्चा की गई है ताकि इन नए फिनफेट-आधारित क्यूडी तकनीकों के साथ डिजाइन की संभावनाओं को पूरी तरह से समझा जा सके। फिनफेट में क्रायोजेनिक तापमान पर क्यूडी प्रदर्शन के कॉमसोल मल्टीफिजिक्स सिमुलेशन भी इस कार्य में प्रस्तुत किए गए हैं ताकि यह प्रदर्शित किया जा सके कि कैसे बॉडी बायस का उपयोग चैनल में बने क्यूडी की चार्ज संवेदनशीलता को ठीक करने के लिए किया जा सकता है। इसके अलावा, मैट्रैब में क्वांटम-गेटेड संचालन को सिमुलेट करने के लिए एक सिलिकॉन स्पिन क्यूबिट के सिमुलेशन के लिए एक कॉम्पैक्ट मॉडलिंग ढाँचा भी प्रस्तुत किया गया है।

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Symbols

ϵ	Dielectric constant/permittivity
ω	Angular frequency
q	Electron charge
$\hbar$	reduced Planck's constant
K_B	Boltzmann constant
I_D	Drain current
I_{TUNNEL}	Tunneling current
$I_{CLASSICAL}$	Classical current
V_{GS}	Gate-to-Source Voltage
V_{DS}	Drain-to-Source Voltage
V_{BS}	Bulk-to-Source Voltage
V_{TH}	Threshold Voltage
E_C	Charging Energy
C_G	Gate-to-QD capacitance
C_D	Drain-to-QD capacitance
C_S	Source-to-QD capacitance
D	Diameter of QD
N_{FIN}	Number of Fins
N_{FINGER}	Number of Fingers
H_{FIN}	Height of Fin
W_{FIN}	Width of Fin
H_{NW}	Height of Nanowire
W_{NW}	Width of Nanowire
μ_{eff}	Effective mobility

Abbreviations

CRF	C entral R esearch F acility
DWLCL	D evice and W afer L evel C haracterization L ab
NISQ	N oisy I ntermediate S cale Q uantum
QPU	Q uantum P rocessing U nit
MuGFET	M ulti- G ate F ield E ffect T ransistor
NWFET	N ano W ire F ield E ffect T ransistor
NSFET	N ano S heet F ield E ffect T ransistor
DGFET	D ouble G ate F ield E ffect T ransistor
SET	S ingle E lectron T ransistor
QDT	Q uantum D ot T hermometer
CBT	C oulomb B lockade T hermometer
QD	Q uantum D ot
LDD	L ightly D oped D rain
RVT	R egular V voltage T hreshold
HVT	H igh V voltage T hreshold
LVT	L ow V voltage T hreshold
SLVT	S uper L ow V voltage T hreshold
SOI	S ilicon O n I nsulator
PSD	P ower S pectral D ensity
SEM	S canning E lectron M icroscope
TEM	T ransmission E lectron M icroscope
GAA	G ate A ll A round
SS	S ubthrehsold S wing
QC	Q uantum C omputer
IC	I ntegrated C ircuits
CNT	C arbon N ano T ube

Abbreviations

SoC	Sy stem on C hip
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