

EFFICIENT VLSI NETWORKS
AND
PARALLEL ALGORITHMS BASED ON THEM

DHRUVA NATH

A thesis submitted to the
Indian Institute of Technology, Delhi
for the award of the degree of

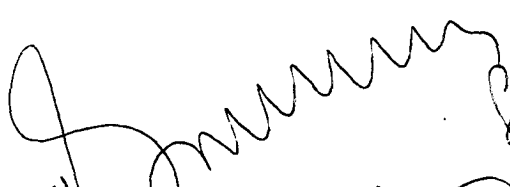
DOCTOR OF PHILOSOPHY

Department of Electrical Engineering
Indian Institute of Technology, Delhi
New Delhi-110016

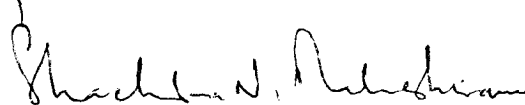
February 1982.

CERTIFICATE

This is to certify that the thesis entitled
'Efficient VLSI Networks And Parallel Algorithms Based
On Them', being submitted by Dhruva Nath to the
Indian Institute of Technology, Delhi for the award
of the degree of Doctor of Philosophy, is a record
of bonafide research work carried out under our
supervision. The results contained in this thesis
have not been submitted to any other University or
Institute for the award of any degree or diploma.



(Prof. F.C.P. Bhatt)



(Prof. S.N. Maheshwari)

Department of Electrical Engg.
Indian Institute of Technology, Delhi
New Delhi-110016.

ACKNOWLEDGEMENTS

- . To Prof.S.N.Maheshwari, for $O(2^n)$ help, guidance, encouragement,....., for creating in me a fascination for the field and for considerably improving my technical writing.
- . To Prof.P.C.P.Bhatt, for all the interest he has taken, for so many long and useful technical discussions, and for going out of his way to help.
- . To Dr.Surendra Prasad, for being so understanding right through.
- . To Prof.S.C.Dutta Roy, whose enthusiasm for teaching and research has been very largely responsible for my decision (the right one) to stick to Academics.
- . To Dr.M.Ibramsha, for some extremely useful discussions, in which I was almost invariably proved wrong.
- . To Anshul, Shashi, Kalra, Murthy, Kumar and Bhalla, for a large number of discussions, at times heated, but always useful.

- . To all the members of the CAD group, for providing a happy and friendly atmosphere to work in, and for relieving me of all additional load when I was fifteen feet deep in my thesis.
- . To Profs. C.D.Thompson, J.L.Bentley and S.R.Kosaraju for some very helpful comments on my work.
- . To Mr.H.L.Narang for an extremely neat and efficient job of typing and to Mr.Amar Singh and Mr.Pandey for carefully bringing this thesis to its final form.
- . I have discovered the perfect little mini-drafter my brother Chicky.
- . And finally, to three very special people, for being just that - very special people.

Dhruva Nath

ABSTRACT

This thesis describes two interconnection networks for parallel processing, namely the Orthogonal Trees Network (OTN) and the Orthogonal Tree Cycles (OTC). Both networks are suitable for VLSI implementation, and are simple to program - visualising algorithms on them is straightforward. While these networks have time performances similar to fast networks such as the Perfect Shuffle Network (PSN) and the Cube Connected Cycles (CCC), they have substantially better Area * time² (AT²) performances for a number of matrix and graph problems. For instance, two NxN Boolean matrices can be multiplied in $O(\log^2 N)$ time on both the OTN and OTC with AT² figures of $O(N^4 \log^2 N)$ on both. Both the CCC and PSN require an AT² of about $O(N^5)$ for this problem. The connected components of an undirected N-vertex graph can be found in $O(\log^3 N \log \log N)$ time on the OTN and OTC, for AT² figures of $O(N^2 \log^8 N \log \log^2 N)$ and $O(N^2 \log^6 N \log \log^2 N)$ respectively. Interestingly, for this problem the time taken is the same as the 'fast-but-large' networks like the PSN and CCC, but the chip area used up is only about as much as the 'slow-but-small' networks like the Mesh. As a result, the AT² figures for the OTN and OTC are substantially better than both: The Mesh, PSN and CCC all require an AT² of about $O(N^4)$ for this problem.

The same is true of the minimal spanning tree problem.

A number of other problems such as sorting and the Discrete Fourier Transform can be solved on the OTN and OTC with AT^2 figures comparable to those of other networks. Therefore, they can be used as general purpose parallel processors. Alternatively, they may be used as special purpose VLSI chips.

CONTENTS

	PAGE NO.
1. <u>INTRODUCTION</u>	1
1.1 Classification Of Parallel Machines	3
1.2 The Shared Memory Machine	4
1.3 Interconnection Networks	5
1.4 Overview Of The Thesis	10
2. <u>THE ORTHOGONAL TREES NETWORK</u>	13
2.1 Structure Of The Orthogonal Trees Network	13
2.2 Operations On The Orthogonal Trees Network	17
2.3 Sorting On The OTN	24
2.4 Matrix Multiplication On The OTN	28
2.5 Graph Algorithms On The OTN	39
2.6 The Simplex Method On The OTN	56
2.7 Divide And Conquer Algorithms On The OTN	60
2.8 Pipelining On The OTN	71
3. <u>THE ORTHOGONAL TREE CYCLES</u>	75
3.1 Structure Of The Orthogonal Tree Cycles	75
3.2 Operations On The Orthogonal Tree Cycles	81
3.3 Sorting On The OTC	89
3.4 Matrix Multiplication On The OTC	95
3.5 Graph Algorithms On The OTC	99
3.6 Discussion	102

	PAGE NO.
4. <u>SOME IMPROVED ALGORITHMS</u>	105
4.1 Graph Algorithms	105
4.2 Combining Different Algorithms	117
4.3 OTN vs OTC - Round 2	130
5. <u>PERFORMANCE EVALUATION OF THE OTN AND OTC</u>	131
5.1 Lower Bounds	131
5.2 Comparison Of The OTN And OTC with Existing Networks	133
5.3 Some Practical Issues	142
6. <u>CONCLUSIONS</u>	145
APPENDIX I . THE VLSI MODEL OF COMPUTATION	148
APPENDIX-II. SOME IMPLEMENTATION DETAILS OF THE OTN AND OTC	150
REFERENCES	160