TUNNEL FIELD EFFECT TRANSISTORS FOR ULTRA-LOW POWER CIRCUITS: DESIGN, SIMULATION AND MODELING

DAWIT BURUSIE ABDI

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY DELHI

DECEMBER 2016

TUNNEL FIELD EFFECT TRANSISTORS FOR ULTRA-LOW POWER CIRCUITS: DESIGN, SIMULATION AND MODELING

by

DAWIT BURUSIE ABDI

Department of Electrical Engineering

Submitted

in fulfilment of the requirements of the degree of Doctor of Philosophy

to the

INDIAN INSTITUTE OF TECHNOLOGY DELHI

DECEMBER 2016

To my mother
Kite

Certificate

This is to certify that the thesis entitled "***Tunnel Field Effect Transistors for Ultra-low Power Circuits: Design, Simulation and Modeling"*** being submitted by **Mr. Dawit Burusie Abdi** for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under my supervision and guidance. The matter embodied in this thesis has not been submitted for the award of any other degree or diploma.

Date:

Place: New Delhi

Dr. Mamidala Jagadesh Kumar

Professor

Department of Electrical Engineering,

Indian Institute of Technology Delhi

New Delhi – 110 016, INDIA

Acknowledgements

First and foremost, I would like to express my sincere gratitude to my advisor Prof. M. Jagadesh Kumar for his continuous support, guidance and enthusiastic encouragement. His suggestions, useful critiques and extensive discussions helped me throughout the time of research and writing of this thesis. Working with him has been the most rewarding experience of my life.

I would also like to thank the members of my thesis committee: Prof. Jayadeva, committee chairman, Dr. Mukul Sarkar, and Dr. Rajendra Singh, for their precious time, insightful comments and encouragement throughout my study. In addition, I am grateful to Dr. Shouri Chatterjee and Prof. Basabi Bhaumik for their help and care during my stay in the institute.

I sincerely acknowledge the Indian Institute of Technology Delhi (IIT Delhi), for providing me the chance to pursue my Ph.D. studies by covering the financial assistance in the form of Institute Scholarship for Ph.D. Assistantship from the program running under memorandum of understanding (MoU) between the Addis Ababa University, Ethiopia and the Indian Institute of Technology Delhi, India, which enabled me to perform my work comfortably. Besides, I am thankful to the Nanoscale Research Facility at IIT Delhi for the additional financial assistance on a number of occasions.

I thank the authorities of Addis Ababa Science and Technology University (AASTU) for granting me a study leave to carry out this Ph.D. work.

Many thanks to the colleagues at AASTU and IIT Delhi for their friendship. I am especially indebted to Anteneh Wodajo at AASTU for his generosity. I am also very thankful to Dhanaraj, Gajendra and all Ethiopian friends at IIT Delhi for the care and

help they provided during my tough times in the first year of stay outside my home country.

I also thank my fellow lab-mates for the stimulating discussions and their help to make my stay in the last four years comfortable. Especially, I am grateful to Sindhu, Avikal, Sumeet, Kanika, Kanan, Rajat, Saketh (now at Technische Universität Chemnitz, Germany) and Pratyush (now at the University of Notre Dame, USA) for the enlightening discussions.

I am also deeply thankful to my childhood friend, Wendimeabezahu Kassahun (Bush), for always being there whenever I needed him.

Last but not the least, I would like to thank my beloved mother, grandmother, brothers and sisters for their unconditional love and affection.

Dawit

Abstract

The significant challenges of power dissipation in scaled down complementary metal oxide semiconductor (CMOS) devices together with the need for long battery life in the growing battery-powered portable devices are driving the research to find alternative switches that (i) overcome the fundamental 60 mV/decade subthreshold swing (SS) limit at room temperature of metal oxide field effect transistors (MOSFETs) and (ii) exhibit low OFF-state current. The tunnel field effect transistor (TFET), which is the focus of this thesis, is one such switch which exhibits both these characteristics due to its band to band tunneling carrier injection mechanism and reverse-biased diode nature, respectively. However, the ON-state current of the TFET is far below that of a MOSFET and furthermore, the TFET is inherently an ambipolar device. These inferior (compared to a MOSFET) and undesired characteristics of a TFET, which affect the performance and may also lead to the malfunctioning of the circuits, limit its application for ultra-low power circuits.

Different TFET designs are being explored to enhance the ON-state current and suppress the ambipolar behavior of a TFET. Introducing a pocket doped region of opposite type to the source dopant next to the source region is among the proposed techniques to enhance the ON-state current and the subthreshold swing of TFET. This structure with introduced pocket doped region is called the PNPN TFET. The introduction of a pocket doped region enhances the electric field at the tunneling junction resulting in a higher ON-state current and a steeper subthreshold slope compared to the conventional p-i-n TFET. However, to achieve these desired characteristics, the doping transition from the source to the pocket region should be

steep and the pocket doped region should be fully depleted. These design constraints make the realization of the ideal pocket region very challenging with current fabrication technologies like ion implantation (for lateral PNPN TFET) and epitaxial growth (for vertical PNPN TFET). Therefore, a technique which eases the realization of the N^+ pocket of the PNPN TFET without the need for a separate implantation or an epitaxial growth is proposed using the charge plasma concept and is investigated using 2D TCAD simulations. Due to the absence of (i) an extra doping step and (ii) complications associated with chemical dopings, the proposed approach overcomes the difficulties of realizing a narrow and fully depleted pocket region of PNPN TFET. The effect of localized charges on the threshold voltage of the PNPN TFET is also analytically modeled and the accuracy of the proposed model is verified by comparing the model results with 2D TCAD simulation results.

Although there are different proposed techniques to suppress the ambipolar conduction of the TFET, none are without their own drawbacks. This absence of an effective and drawback free suppression technique makes the choice of one technique over the other to depend on the specific requirement of the application and thus, calls for the investigation of additional ambipolar suppression techniques. In this thesis, therefore, two techniques are proposed and investigated. These are (i) the overlapping gate-on-drain and (ii) the dual material gate (DMG). The former limits the gate to control the tunneling barrier width only at the source-channel interface irrespective of the polarity of the gate voltage and the latter divides the channel into two regions so that it is possible to control the proportion of the accumulated holes in each region which then reduces the tunneling at the drain-channel junction. In addition, the possibility of using the overlapped gate-on-drain structure as a biosensor is examined using 2D TCAD simulations.

Table of Contents

List of Figures

List of Symbols

AG	Auxiliary Gate
BGN	Band Gap Narrowing
BTBT	Band To Band Tunneling
CMOS	Complementary Metal Oxide Semiconductor
DMG	Dual Material Gate
E_g	Energy band gap of the material
GDU	Gate Drain Underlap
IC	Integrated Circuit
$I_{DS,subthreshold}$	Subthreshold current
I_{OFF}	OFF-State current
I_{ON}	ON-State current
K	Dielectric constant
L	Channel length
L_{AG}	Length of auxiliary gate
L_d	Length of damaged region
L_{gap}	Gate-drain electrode gap
L_{N+}	N^+ pocket length
L_{ov}	Gate on drain overlap length
L_{UD}	Length by which the gate is shortened on the drain side (i.e. underlap region)

L_t	Minimum tunneling length
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
m^*	Effective carrier mass
m_o	Free electron mass
N_f	Interface charge density
SMG	Single Material Gate
SS	Subthreshold Swing
TFET	Tunnel Field Effect Transistor
TG	Tunneling Gate
t_{ox}	Gate oxide thickness
t_{si}	Silicon body thickness
V_{DD}	Supply voltage
V_{FB}	Flat band voltage
V_{FB0}	Flat band voltage without interface charges
V_{th}	Threshold voltage
ε_{ox}	Dielectric constant of oxide
ε_{Si}	Dielectric constant of silicon
$\Delta\Phi$	Energy range over which tunneling takes place
Φ_{AG}	Work function of auxiliary gate
Φ_{TG}	Work function of tunnel gate