

**“DESIGN AND ANALYSIS OF EMERGING
NANOSCALE MOSFETS FROM LOW-POWER AND
HIGH-SPEED PERSPECTIVE**

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HIGH-SPEED PERSPECTIVE**

by

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Submitted

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*Dedicated to
Aajoba, Aaji, Aai, Baba, Kaka, Kaku, Yogita and all the teachers whom I came across at different
stages during the last 29 years of my life. Some motivated me, some inspired me, some helped in
designing the process flow of my life, often poking me with a sharp stick called “truth”, enabling my
fabrication in the present form.*

Certificate

This is to certify that the thesis entitled “**Design and Analysis of Emerging Nanoscale MOSFETs From Low-Power and High-Speed Perspective**” being submitted by **Mr. Gaurav Musalgaonkar** for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under my supervision and guidance. The matter embodied in this thesis has not been submitted for the award of any other degree or diploma.

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Abstract

The ever-increasing demand for multiple functionalities in the mobile gadget has led to an incessant scaling of the MOSFETs. Although device scaling improves the speed, drive current, and reduces the dynamic power dissipation, the consequent short channel effects (SCEs) increase the static power dissipation significantly. Moreover, the inability to scale down the sub-threshold swing (SS) below 60 mV/decade also known as Boltzmann tyranny due to the inherent thermionic injection mechanism of conduction in conventional MOSFETs makes it difficult to scale down the supply voltage.

Various multi-gate architectures such as FinFETs, Nanowire (NW) FETs, and Nanotube (NT) FETs were proposed to minimize the SCEs in order to continue the scaling of MOSFETs in nanoscale regime. However, they failed to reduce the SS below the conventional limit of 60 mV/decade due to the Boltzmann tyranny arises out of the inherent thermionic transport mechanism of the MOSFETs. As a result, at the lower technology nodes, inability to scale the supply voltage continues to limit the scaling of multi-gate architectures. Therefore, as an alternative, various device architectures with different transport mechanisms such as band-to-band tunneling (BTBT) and impact ionization have been suggested to reduce the SS below the conventional limit of 60 mV/decade. Finally, in the pursuit of achieving both, i.e. best electrostatic control, and sub-60 mV/decade of SS for the next generation low power, high speed devices, 3D device architecture with alternate conduction mechanism has been extensively investigated.

The tunnel field-effect transistor (TFETs), which employs BTBT as the conduction mechanism to inject carriers in the channel and the impact-ionization MOS (I-MOS) which relies on the impact ionization phenomena for conduction in contrast to the carriers injection by thermal injection in MOSFETs. These devices are regarded as one of the most promising alternatives for ultra-low power integrated circuits (ICs) owing to the minimized SCEs, ultra-low leakage current due to reverse biased p-i-n structure, and steep turn-on characteristics even at low supply voltages.

Although, TFETs and I-MOS offer steep SS compared to the conventional MOSFETs, there are few challenges that need to be addressed carefully in order to achieve the maximum

benefits from these devices. For example, in TFET, the low drive current obtained due to its conduction mechanism of BTBT in the ON-state is still a major bottleneck. Similarly, in I-MOS, a higher breakdown voltage makes it unsuitable for low power logic applications. Therefore, unless these obstacles are overcome, we cannot deploy these architectures in the mainstream CMOS technology.

Therefore, in this thesis, we have proposed various solutions to improve the ON-state current and to achieve steep switching in the emerging nanotube tunnel FETs for the next generation low-power and high-speed devices in sub-10 nm technology nodes. Furthermore, we have also proposed a solution to reduce the breakdown voltage in I-MOS.

First, a solution is proposed to lower the breakdown voltage in I-MOS. This is based on a deliberate misalignment between the top and bottom gates in a double gate I-MOS to achieve sub-1.0 V breakdown voltage for low power and high-speed applications.

The efficacy of misaligned core-gate and shell-gate architecture in nanotube to improve the area for line tunneling is also analyzed for the first time. Unlike the conventional NT-TFETs with only point tunneling mechanism, in the proposed solution, both line and point tunneling take place resulting in the improved ON-state current.

Furthermore, nanotube TFET architecture is explored for future ultra-low power applications. A nanotube with core-source is proposed where the entire tunneling path is aligned with the direction of gate electric field, known as line tunneling. The proposed solution exhibits a steep subthreshold swing (SS_{avg}) of 33 mV/decade over more than 8 decades of current change and ~6 times higher drain compared to the conventional NT-TFET for a supply voltage of 0.3 V.

Since, TFETs scaling at lower technology nodes require ultra-steep doping profiles at the source-channel tunnel junction. However, realizing abrupt junction with ultra-steep doping profiles requires low thermal budget while achieving high dopant activation in the degenerate source and drain regions in TFET demands a high temperature annealing which may lead to source/drain dopant diffusion into the channel region. Therefore, this complex and conflicting constraint on the thermal budget makes it difficult to realize abrupt doping profiles and limits the tunneling efficiency in p-i-n TFETs at smaller technology nodes. Therefore, we propose a novel PNNT-TFET architecture without the need for any abrupt source-channel tunnel junction. The

proposed p-n junction NT-TFET uses a dual metal gate (DMG) to induce the tunneling junctions thus mitigating the need of abrupt source-channel tunnel junction doping.

सार

मोबाइल गैजेट में कई प्रकार की कार्यक्षमता के लिए बढ़ती मांग के कारण MOSFETs की संख्या में निरंतर वृद्धि हुई है। यद्यपि डिवाइस स्केलिंग गति में सुधार करता है, वर्तमान ड्राइव करता है, और dynamic power अपव्यय को कम करता है, परिणामी लघु चैनल प्रभाव (SCEs) static power अपव्यय को काफी बढ़ाता है। इसके अलावा, पारंपरिक MOSFETs में subthreshold slope को 60 mV / decade से नीचे करने में असमर्थता कारण, जो की बोल्टज़मैन tyranny की वजह से थर्मिओनिक चलन तंत्र की वजह से उत्पन्न होता है ।

FinFETs, Nanowire (NW) FETs, और Nanotube (NT) FETs जैसे कई मल्टी-गेट आर्किटेक्चर, SCEs को कम करने के लिए प्रस्तावित किए गए ताकि MOSFETs की स्केलिंग को जारी रखा जा सके। हालांकि, वे 60 mV/ दशक की पारंपरिक सीमा से नीचे SS को कम करने में विफल रहे जिसका कारण MOSFET में अंतर्निहित थर्मियोनिक परिवहन तंत्र बोल्टज़मैन tyranny है । नतीजतन, कम प्रौद्योगिकी नोड्स पर, आपूर्ति वोल्टेज को स्केल करने में असमर्थता मल्टी-गेट आर्किटेक्चर की स्केलिंग को सीमित करने के लिए जारी है। इसलिए, एक विकल्प के रूप में, विभिन्न परिवहन तंत्र जैसे बैंड-टू-बैंड टनलिंग (बीटीबीटी) और प्रभाव आयनीकरण (Impact Ionization) के साथ विभिन्न डिवाइस आर्किटेक्चर को उपयोग करके SS को 60 mV/ दशक की पारंपरिक सीमा से कम करने का सुझाव दिया गया है। अंत में, दोनों को प्राप्त करने की खोज में, अर्थात् सबसे अच्छा इलेक्ट्रोस्टैटिक नियंत्रण, और अगली पीढ़ी के लिए का उपयोग कम बिजली

लिए का उपयोग, उच्च गति वाले उपकरणों के लिए SS के 60 mV/ दशक, वैकल्पिक चालन तंत्र के साथ 3D डिवाइस आर्किटेक्चर की बड़े पैमाने पर जांच की गई है।

टनल FET ट्रांजिस्टर (TFETs), जो चैनल में वाहक इंजेक्शन करने के लिए प्रवाहकत्व तंत्र के रूप में BTBT को नियोजित करता है और प्रभाव-आयनीकरण (Impact Ionization) MOS (I-MOS) जो वाहक इंजेक्शन के विपरीत चालन के लिए प्रभाव आयनिकरण घटना पर निर्भर करता है। इन उपकरणों को अल्ट्रा-लो पावर एकीकृत सर्किट के लिए सबसे आशाजनक विकल्पों में से एक के रूप में माना जाता है, जो कि कम से कम SCEs, अल्ट्रा-कम लीकेज करंट के कारण होता है, जो की p-i-n डायोड संरचना के कारण होता है, और कम आपूर्ति वाले वोल्टेज पर भी स्टेप टर्न-ऑन विशेषताओं के कारण होता है।

हालाँकि, TFET और I-MOS पारंपरिक MOSFETs की तुलना में तीव्र SS की पेशकश करते हैं, लेकिन इन वास्तुशिल्प से अधिकतम लाभ प्राप्त करने के लिए कुछ चुनौतियों का सामना सावधानी से करने की आवश्यकता है। उदाहरण के लिए, TFET में, ऑन-स्टेट में BTBT के अपने चालन तंत्र के कारण कम ड्राइव करंट प्राप्त होता है , जो की अभी भी एक बड़ी अड़चन है। इसी तरह, I-MOS में, एक उच्च ब्रेकडाउन वोल्टेज कम वोल्टेज के अनुप्रयोगों के लिए अनुपयुक्त बना देता है। इसलिए, जब तक इन बाधाओं को दूर नहीं किया जाता है, हम इन आर्किटेक्चर को मुख्य धारा CMOS प्रौद्योगिकी में तैनात नहीं कर सकते हैं

इसलिए, इस थीसिस में, हमने ON-state करंट में सुधार करने और अगली पीढ़ी के कम-पावर और उच्च गति वाले उपकरणों के लिए उप-10 नैनो मीटर प्रौद्योगिकी नोड्स में उभरते नैनोट्यूब टनल FETs में तीव्र स्विचिंग प्राप्त करने के लिए विभिन्न समाधानों का प्रस्ताव किया है। इसके अलावा, हमने I-MOS में ब्रेकडाउन वोल्टेज को कम करने के लिए एक समाधान भी प्रस्तावित किया है।

सबसे पहले, I-MOS में ब्रेकडाउन वोल्टेज को कम करने के लिए एक समाधान प्रस्तावित है। यह कम बिजली और उच्च गति वाले अनुप्रयोगों के लिए उप-1.0 V ब्रेकडाउन वोल्टेज को प्राप्त करने के लिए एक डबल गेट I-MOS में ऊपर और नीचे के फाटकों के बीच एक जानबूझकर मिसलिग्न्मेंट पर आधारित है।

इसके अलावा, उभरते नैनोट्यूब TFET आर्किटेक्चर को भविष्य की कम-शक्ति और उच्च गति वाले अनुप्रयोगों के लिए खोजा गया है। कोर-सोर्स वाला एक नैनोट्यूब प्रस्तावित है जहां टनलिंग पथ को गेट इलेक्ट्रिक फ़ील्ड की दिशा के साथ संरेखित किया जाता है, जिसे लाइन टनलिंग के रूप में जाना जाता है।

इस थीसिस में प्रस्तावित Nanotube समाधान, पारम्परिक Nanotube के मुकाबले 6 गुना अधिक करंट प्रवाह करता है। इसके अतिरिक्त इसमें बहुत की काम ऊर्जा की खपत होती है ($V_{GS} = V_{DS} = 0.3 \text{ V}$)। ये बहुत ही काम SS 33 mv/ दशक प्रदर्शित करता है

नैनोट्यूब में लाइन टनलिंग के लिए क्षेत्र में सुधार करने के लिए नैनोट्यूब में असंरेखित कोर-गेट और शेल-गेट आर्किटेक्चर की प्रभावशीलता का भी पहली बार विश्लेषण किया गया है। प्रस्तावित समाधान में केवल बिंदु टनलिंग तंत्र के साथ पारंपरिक NT-TFETs के विपरीत, दोनों लाइन और बिंदु टनलिंग में सुधार होता है जिसके परिणामस्वरूप ON-state करंट में सुधार होता है।

इसके अलावा, कम प्रौद्योगिकी वाले नोड्स में TFET स्केलिंग के लिए तीव्र डोपिंग प्रोफाइल की आवश्यकता होती है। हालांकि, अल्ट्रा-स्टॉप डोपिंग प्रोफाइल के साथ तीव्र जंक्शनों को साकार करने के लिए काम थर्मल स्रोत की आवश्यकता होती है। जबकि उच्च डोपेंट सक्रियण प्राप्त करने के लिए काम थर्मल बजट की आवश्यकता होती है |और TFET में तीव्र जंक्शनों को साकार करने channel क्षेत्र एक उच्च तापमान की मांग करता है जिससे चैनल क्षेत्र में source/channel डोपिंग प्रसार हो सकता है। इसलिए, थर्मल बजट पर इस जटिल और परस्पर विरोधी बाधा को तीव्र डोपिंग प्रोफाइल को प्राप्त करना मुश्किल हो जाता है और ये p-i-n TFET में टनलिंग दक्षता को सीमित करता है।

इसलिए, हम किसी भी तीव्र source/channel tunnel जंक्शन की आवश्यकता के बिना एक नए PNNT-TFET वास्तुकला का प्रस्ताव करते हैं। प्रस्तावित पी-एन जंक्शन एनटी-टीएफईटी एक दोहरी धातु गेट (डीएमजी) का उपयोग करता है ताकि टनलिंग जंक्शनों को प्रेरित किया जा सके और इस प्रकार तीव्र स्रोत-चैनल टनल जंक्शन डोपिंग की आवश्यकता को कम किया जा सके।

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List of Symbols

CMOS	Complementary Metal Oxide Semiconductor
MOSFET	METAL Oxide Semiconductor Field Effect Transistor
TCAD	Technology Computer Aided Design
IC	Integrated Circuit
II	Impact Ionization
BTBT	Band-to-Band-Tunneling
SCEs	Short Channel Effects
DIBL	Drain Induced Barrier Lowering
DIBT	Drain Induced Barrier Thinning
I_{OFF}	Drain current at zero gate voltage
I_{ON}	Drain current at gate voltage equal to supply voltage
V_{DD}	Supply Voltage
K	Dielectric Constant of insulator material
EG	Energy Bandgap of the material
EOT	Effective Oxide Thickness of Gate Insulator
SOI	Silicon on Insulator
DMG	Dual Metal Gate
SMG	Single Metal Gate
TFET	Tunnel Field Effect Transistor
IMOS	Impact Ionization Metal Oxide Semiconductor
M-IMOS	Misaligned Impact Ionization Metal Oxide Semiconductor
JLFET	Junctionless Field Effect Transistor

NCFET	Negative Capacitance Field Effect Transistor
FBFET	Feedback Field Effect Transistor
NTTFET	Nanotube Field Effect Transistor
MGNT	Misaligned Gate Nanotube
CSNT	Core-Source Nanotube
PNNTTFET	p-n Junction Nanotube Tunnel Field Effect Transistor
T_{si}	Thickness of Active Silicon Layer
T_{OX}	Gate Oxide Thickness
V_{SD}	Source-to-Drain Voltage
V_{GD}	Gate-to-Drain Voltage
L_{G1}	Top-Gate Length
L_{G2}	Bottom-Gate length
L_{I1}	Upper Intrinsic Region Length
L_{I2}	Bottom Intrinsic Region Length
L_{SP}	Length of The Spacer Region
V_{BD}	Avalanche Breakdown Voltage
V_{TH}	Threshold Voltage
α_n	Electron Impact Ionization Rate
α_p	Hole Impact Ionization Rate
A_N	Electron Impact Ionization Coefficient
A_P	Hole Impact Ionization Coefficient
B_N	Electron Impact Ionization Coefficient
B_P	Hole Impact Ionization Coefficient
ξ	Electric Field
MN	Smoothing Parameter
MP	Smoothing Parameter
SS	Subthreshold Swing
NW	Nanowire

GAA	Gate-All-around
EBL	Electron Beam lithography
LPCVD	Low Pressure Chemical Vapor Deposition
TEOS	Tetraethyl Orthosilicate
ALD	Atomic Layer Deposition
C_{GG}	Total Gate Capacitance
C_{GD}	Gate-to-Drain Capacitance
ϕ_{GC}	Core-Gate Work Function
ϕ_{GS}	Shell-Gate Work Function
L_{OV}	Length of Source Overlapped Core-Gate
d_{core}	Core-Gate Diameter
TAT	Trap Assisted Tunneling
DSDT	Direct Source-to-Drain Tunneling
SGSO	Shell-Gate Source Overlapped
CGSO	Core-Gate Source Overlapped
V_{ON}	Gate Voltage at which the Drain Current Rises Sharply
L_{DEXT}	Source-Drain Spacer Extension length
EDP	Energy Delay Product
ϕ_{CON}	Control gate Work Function
ϕ_{TUN}	Tunneling Gate Work Function
X_J	Doping gradient
L_{TUN}	Tunneling Distance
QC	Quantum Confinement
CPP	Contacted Poly Pitch