HIGH-VOLTAGE THIN-FILM LATERAL BIPOLAR TRANSISTOR CONCEPTS ON SOI: A SIMULATION STUDY

by

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Submitted

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to the

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Dedicated to my Mother

Certificate

This is to certify that the Thesis entitled **"High-Voltage Thin-film Lateral Bipolar Transistor Concepts on SOI: A Simulation Study"** being submitted by **Sukhendu Deb Roy** to the **Indian Institute of Technology Delhi**, for the award of the degree of **Doctor of Philosophy** in **Electrical Engineering** is a bona fide work carried out by him under my supervision. The work reported in this thesis, in my view has reached the magnitude and standard for submission and for staking the candidate's claim for the award of Ph.D Degree in Engineering. The research reports and the results presented in this thesis have not been submitted in parts or in full to any other University or Institute for the award of any other degree or diploma.

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Abstract

Silicon-On-Insulator (SOI) is a technological innovation that provides superior isolation with low leakage current and makes possible designing high voltage lateral devices. Currently advanced Bipolar Complementary Metal Oxide Semiconductor (BiCMOS) and Double Diffused MOS (DDMOS) devices on SOI are of great interest for their applications in high speed digital, analog and power integrated circuits. However, with continuous trend towards reducing SOI film thickness, on-resistance, power dissipation and self-heating of the SOI power MOSFETs are becoming serious concerns as they increase in proportion to the blocking voltage.

On the other hand, the compatibility of a thin-film Lateral Bipolar Transistors (LBT) with the BiCMOS processes on SOI and its conductivity modulation property makes it attractive for low and medium voltage applications. With this motivation, thin-film (0.2 μm) Lateral Bipolar Transistor (LBT) and Schottky Collector Lateral Bipolar Transistor (SCBT) structures on SOI have been studied by using two dimensional numerical process and device simulators (ATHENA and ATLAS) for their possible applications in automotive, mixed signal and Power Integrated Circuits (PICs) or to serve as alternatives for the conventional or new generation thin-film power MOSFETs.

However, by using conventional design principles, it is difficult to realize the thin-film LBT structures on SOI that show high breakdown voltage, reduced quasi-saturation and self-heating effect. The present work, therefore, introduces a few new and novel thin-film LBT and SCBT structures on SOI and Partial SOI (PSOI) technologies to realize this trade-off. The improved characteristics of the new structures have been analyzed and

compared with their respective conventional LBT and lateral SCBT structures on SOI. The new LBT and SCBT design concepts proposed in this study are:

[a] a new Collector-Tub three-zone Step doped Lateral Bipolar Transistor (CT-SLBT) structure that combines the Collector-Tub (CT) and three-zone step doped charge profile, thereby improving the breakdown voltage by about 80%, as compared to that of the conventional LBT on SOI. The improved characteristics of the new CT-SLBT structure is expected to alleviate the trade-off between the high breakdown voltage and reduced self-heating effect in thin-film LBT on SOI and find applications in analog and power integrated circuits.

[b] a new high voltage Vertical submicron BJT on SOI with three-zone Step doped Lateral Collector (VSLC) structure that is expected to solve (a) the problem of defining the base region, (ii) use a highly doped base region to reduce the base-width modulation effect, and (iii) show about 60% improvement in the breakdown voltage due to the RESURF effect of the three-zone step doped doping profile.

[c] a novel high voltage two-zone base Extended BOX Schottky Collector Bipolar Transistor (TESCBT) structure on SOI that comprises a highly doped base and a lightly doped base, and an extended BOX. The combined effect has been shown to enhance the breakdown voltage to about 29.0 V, and is, so far, the highest reported breakdown voltage on 0.2 μm thin-film SCBT over 0.2 μm BOX. Also, a two-zone base thin-film SCBT on Partial SOI (PSOI) has been proposed for reducing the steady state temperature in the device.

The dissertation also contains a few proposals for extending the scope of this study for further exploitation.

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