

INNOVATIVE ADVANCEMENTS IN ANTI-ISLANDING PROTECTION FOR ENHANCED POWER QUALITY AND MINIMAL NDZ

RAKESH SHAMRAO PATEKAR



**DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY DELHI
MARCH 2025**

© Indian Institute of Technology Delhi (IITD), New Delhi, 2025

**Innovative Advancements in Anti-Islanding Protection for
Enhanced Power Quality and Minimal NDZ**

by

RAKESH SHAMRAO PATEKAR

Department of Electrical Engineering

Submitted

*In fulfillment of requirements of degree of **Doctor of Philosophy***

to the



**INDIAN INSTITUTE OF TECHNOLOGY DELHI
HAUZ KHAS, NEW DELHI-110016, INDIA
MARCH, 2025**

*This thesis is dedicated to my late father,
Shree Shamrao Dadaji Patekar*

CERTIFICATE

This is to certify that the thesis entitled '**Innovative Advancements in Anti-Islanding Protection for Enhanced Power Quality and Minimal NDZ**', being submitted by **Rakesh Shamrao PATEKAR** to **Indian Institute of Technology, Delhi** is a record of bonafide research work carried out under my supervision and I consider it worthy for consideration of the award of the degree **Doctor of Philosophy** in Electrical Engineering. The results obtained here have not been submitted to any other University or Institute for the award of any degree or diploma.

Prof. Bijaya Ketan Panigrahi

Department of Electrical Engineering,

Indian Institute of Technology Delhi,

New Delhi - 110016, India.

Date:

Place:

Acknowledgments

To my Supervisor: I sincerely thank my supervisor, Prof. B. K. Panigrahi, for his consistent support, guidance, and encouragement throughout my research journey. Prof. Panigrahi's expertise, enthusiasm for the subject, and knack for simplifying complex concepts have significantly enriched my understanding. His willingness to grant me independence in my research empowered me to explore deeply and broadly across different domains. His mentorship has been instrumental in shaping my growth and accomplishments in this field.

To my research committee members and teachers during my coursework: I sincerely thank my doctoral research committee members, Prof. N. Senroy, Prof. A. R. Abhyankar, and Prof. A. Verma, for their invaluable guidance and feedback in shaping my research direction. I thank esteemed teachers like Prof. S. Mishra and Prof. S. Bhasin for enriching my coursework. I want to especially thank Dr. Rabindra Mohanty for sharing his knowledge and contributing to my PhD journey.

To all my past teachers: I extend my heartfelt appreciation to my former educators from school, college, and coaching institutes, whose guidance and mentorship equipped me to pursue this esteemed degree. I extend my heartfelt gratitude to my esteemed teachers, Mr. Rupesh Ghagi, Mr. Ganesh Pawde, Mr. Yogesh Dhumne, Mr. Sandip Dakhre, Mr. M. Petkar, Mr. Rakhe, Mr. Kawalkar, Mr. Dhanegaonkar, and Mr. Chikhlikar, for their constant support during the early stages of my life. Their encouragement ignited my passion for education and life.

To my financial Stakeholders: I also thank the Ministry of Human Resource Development (MHRD), Government of India, for providing financial support through a scholarship to complete the Doctoral program at IIT Delhi.

To my professors from past institutes: I sincerely thank all the professors who have supported me directly or indirectly during my graduation and post-graduation education. I sincerely thank Prof. S. R. Tambay, Prof. A. Mitra, Prof. P. Kulkarni, and Prof. M. Ballal for their constant support during my master's thesis. I also want to thank my B. Tech supervisors, Prof. S. M. Shinde, Prof. A. Thoasr, Prof. A. Bhole, and all the professors at GECA Aurangabad.

To my late father: This thesis is dedicated to my late father, Shree Shamrao Dadaji Patekar, who believed in me and supported my education. His thoughts on education have allowed me to become who I am today. He is my inspiration to work hard and achieve such a great position. Thank you so much for your support throughout my entire life. I only regret that you are no longer here to see my success.

To my family members: I am deeply thankful to my mother, Mrs. Indu Shamrao Patekar; my brother, Vaibhav Patekar; my wife, Mrs. Rohini Rakesh Patekar; and my extensive family for their invaluable upbringing, sacrifices, and unwavering support, without which my education wouldn't have been possible.

To my friends, Seniors, and my extended researcher family: I am deeply thankful to my seniors, Dr. Diptak Pal and Dr. Pankaj Achlerkar, for their constant support and motivation during my PhD journey. I also want to thank Miss Arjita Pal for her continuous support and help. I am grateful to all the seniors, colleagues, and juniors who assisted me directly or indirectly throughout my PhD journey.

— RAKESH SHAMRAO PATEKAR

Abstract

Emerging challenges in anti-islanding protection systems have arisen due to increased load diversity and the widespread adoption of Inverter-Based Generation (IBG) within the electrical power distribution system (EPDS). Integrating distributed generators (DGs) with advanced anti-islanding protection systems (AIPS) is essential to guarantee operational integrity, particularly for IBGs in distribution networks. Nevertheless, conventional AIPS often fail to detect unintentional islanding events during perfectly matched loading conditions, highlighting a critical vulnerability. Furthermore, most IBGs employ active islanding detection strategies due to their minimal non-detection zone (NDZ) and rapid response. However, the power quality of the distribution network may suffer due to the increasing penetration of the active disturbance signals. Load diversity also plays an essential role in analyzing the NDZ and detection time of AIPS. The impact of load diversity on NDZ and the detection time of AIPS is significant, highlighting the need for comprehensive analysis in scientific literature. Therefore, it is crucial for the scientific community to thoroughly examine a range of diverse load models and their effects on islanding detection techniques.

The thesis proposes a novel solution to overcome the aforementioned challenges by introducing a new AIPS with zero non-detection zone (NDZ), characterized by rapid operation and minimal impact on power quality, robustness, and reliability. Additionally, it includes a comprehensive study focusing on load diversity and parameter settings. The thesis thoroughly discusses its contributions in detail, focusing on the following aspects.

- A hybrid islanding detection algorithm is introduced, leveraging both the rate of change of kinetic energy and the root-mean-square value of absolute frequency deviation at the point of common coupling (PCC). This methodology represents a notable advancement over existing techniques, particularly regarding the injection mechanism of disturbances via the q-axis current control loop of the grid-tied inverter. The algorithm activates the disturbance signal injection mechanism solely when an unintentional islanding event is anticipated, as determined by monitoring specific parameters at the PCC. This mechanism is proposed to

achieve zero non-detection zones, operate with remarkable speed, have a straightforward implementation process, and exert significantly less impact on the power quality and stability of the power electronics system.

- A thorough analysis of diverse load models, including emerging electric vehicle (EV) charging loads, and their effects on non-detection zones has been conducted. Different load models and their impact on overfrequency, underfrequency, overvoltage, and undervoltage protection schemes have been examined under varying EV charging load penetration levels.
- The study investigates the impact of different islanding detection methods on power quality. Moreover, it assesses the current signal's total harmonic distortion (THD) concerning parameter variations across various islanding detection methods. This comparative analysis offers valuable insights for improving islanding detection methods to mitigate their effects on power quality.
- The proposed AIPS architecture has undergone rigorous real-time testing in various scenarios using both the Typhoon-hardware-in-loop (HIL) and the real-time digital simulator (RTDS) based power hardware in the loop (PHIL) testbed. The performance of the method has been assessed through over 200 islanding and non-islanding case studies in simulation and experimental settings. Results indicate that the proposed method is robust, accurate, and capable of detecting islanding events swiftly, with a detection time as short as 150 milliseconds.

Key Words: Distributed generation (DG), Disturbance injection, Islanding identification, Non-detection zones(NDZ), Power quality, Protection, Rate of change of kinetic energy (ROCOKE), Real-time digital simulator (RTDS), Typhoon hardware-in-loop (HIL).

सार (Abstract)

भार विविधता में वृद्धि और विद्युत शक्ति वितरण प्रणाली के भीतर इनवर्टर-आधारित उत्पादन को व्यापक रूप से अपनाने के कारण एंटी-आइलैंडिंग सुरक्षा प्रणालियों में उभरती चुनौतियां उत्पन्न हुई हैं। विशेष रूप से वितरण नेटवर्क में आईबीजी के लिए परिचालन अखंडता की गारंटी के लिए उन्नत एंटी-आइलैंडिंग प्रोटेक्शन सिस्टम (एआईपीएस) के साथ वितरित जनरेटर को एकीकृत करना आवश्यक है। फिर भी, पारंपरिक एआईपीएस अक्सर पूरी तरह से मेल खाने वाली लोडिंग स्थितियों के दौरान अनजाने में द्वीप की घटनाओं का पता लगाने में विफल रहता है, जो एक महत्वपूर्ण भेद्यता को उजागर करता है। इसके अलावा, अधिकांश आईबीजी अपने न्यूनतम गैर-पहचान क्षेत्र और त्वरित प्रतिक्रिया के कारण सक्रिय द्वीप का पता लगाने की रणनीतियों को नियोजित करते हैं। हालांकि, सक्रिय विक्षोभ संकेतों के बढ़ते प्रवेश के कारण वितरण नेटवर्क की बिजली की गुणवत्ता प्रभावित हो सकती है। भार विविधता एन. डी. जेड. के विश्लेषण और ए. आई. पी. एस. के पता लगाने के समय में भी एक आवश्यक भूमिका निभाती है। एनडीजेड पर भार विविधता का प्रभाव और एआईपीएस का पता लगाने का समय महत्वपूर्ण है, जो वैज्ञानिक साहित्य में व्यापक विश्लेषण की आवश्यकता को उजागर करता है। इसलिए, वैज्ञानिक समुदाय के लिए यह महत्वपूर्ण है कि वे विभिन्न भार मॉडलों की एक श्रृंखला और द्वीप का पता लगाने की तकनीकों पर उनके प्रभावों की अच्छी तरह से जांच करें।

यह शोध प्रबंध शून्य गैर-पहचान क्षेत्र के साथ एक नया एआईपीएस शुरू करके उपरोक्त चुनौतियों को दूर करने के लिए एक नए समाधान का प्रस्ताव करता है, जिसमें तेजी से संचालन और बिजली की गुणवत्ता, मजबूती और विश्वसनीयता पर न्यूनतम प्रभाव होता है। इसके अतिरिक्त, इसमें भार विविधता और पैरामीटर सेटिंग्स पर ध्यान केंद्रित करने वाला एक व्यापक अध्ययन शामिल है। इस शोध प्रबंध में निम्नलिखित पहलुओं पर ध्यान केंद्रित करते हुए इसकी समस्याओं पर विस्तार से चर्चा की गई है।

- एक हाइब्रिड आइलैंडिंग डिटेक्शन एल्गोरिथ्म पेश किया गया है, जो सामान्य युग्मन के बिंदु पर गतिज ऊर्जा के परिवर्तन की दर और निरपेक्ष आवृत्ति विचलन के मूल-अर्थ-वर्ग मूल्य दोनों का लाभ उठाता है। यह पद्धति मौजूदा तकनीकों पर एक उल्लेखनीय प्रगति का प्रतिनिधित्व करती है, विशेष रूप से ग्रिड-टाईड इन्वर्टर के क्यू-एक्सिस करंट कंट्रोल लूप के माध्यम से गड़बड़ी के इंजेक्शन तंत्र के संबंध में। एल्गोरिथ्म विक्षोभ संकेत इंजेक्शन तंत्र को केवल तभी सक्रिय करता है जब एक अनजाने में द्वीप की घटना का अनुमान लगाया जाता है, जैसा कि पीसीसी में विशिष्ट मापदंडों की निगरानी द्वारा निर्धारित किया जाता है। यह तंत्र शून्य गैर-पहचान क्षेत्रों को प्राप्त करने, उल्लेखनीय गति के साथ संचालित करने, एक सीधी कार्यान्वयन प्रक्रिया रखने और बिजली की गुणवत्ता और बिजली इलेक्ट्रोनिक्स प्रणाली की स्थिरता पर काफी कम प्रभाव डालने के लिए प्रस्तावित है।
- उभरते इलेक्ट्रिक वाहन (ईवी) चार्जिंग लोड सहित विभिन्न लोड मॉडलों और गैर-पहचान क्षेत्रों पर उनके प्रभावों का गहन विश्लेषण किया गया है। विभिन्न लोड मोड-एल्स और ओवर-फ्रीक्वेंसी, अंडर-फ्रीक्वेंसी, ओवर-वोल्टेज और अंडर-वोल्टेज सुरक्षा योजनाओं पर उनके प्रभाव की जांच अलग-अलग ईवी चार्जिंग लोड प्रवेश स्तरों के तहत की गई है।
- अध्ययन शक्ति गुणवत्ता पर विभिन्न द्वीपीय पहचान विधियों के प्रभाव की जांच करता है। इसके अलावा, यह विभिन्न द्वीपीय पहचान विधियों में पैरामीटर भिन्नताओं के संबंध में वर्तमान संकेत की कुल हार्मोनिक विकृति (टीएचडी) का आकलन करता है। यह तुलनात्मक विश्लेषण बिजली की गुणवत्ता पर उनके प्रभावों को कम करने के लिए द्वीपों का पता लगाने के तरीकों में सुधार के लिए मूल्यवान अंतर्दृष्टि प्रदान करता है।
- उन्होंने प्रस्ताव दिया एआईपीएस आर्किटेक्चर का टाइफून-हार्डवेयर-इन-लूप (एचआईएल) और रियल-टाइम डिजिटल सिमुलेटर (आरटीडीएस) आधारित पावर हार्डवेयर इन द लूप (पीएचआईएल) टेस्टबेड दोनों का उपयोग करके विभिन्न क्षेत्रों में कठोर रियल-टाइम परीक्षण किया गया है। सिमुलेशन और प्रयोगात्मक सेटिंग्स में 200 से अधिक आइलैंडिंग और गैर-आइलैंडिंग केस स्टडी के माध्यम से विधि के प्रदर्शन का मूल्यांकन किया गया है। परिणाम इंगित करते हैं कि प्रस्तावित विधि मजबूत, सटीक और द्वीप की घटनाओं का तेजी से पता लगाने में सक्षम है, जिसका पता लगाने का समय 150 मिलीसेकंड जितना कम है।

मुख्य शब्द: डिस्ट्रिब्यूटेड जेनरेशन (डीजी), डिस्टर्बेस इंजेक्शन, आइलैंडिंग आइडेंटिफिकेशन, नॉन-डिटेक्शन जोन (एनडीजेड), बिजली की गुणवत्ता, सुरक्षा, गतिज ऊर्जा के परिवर्तन की दर, रियल-टाइम डिजिटल सिमुलेटर (आरटीडीएस), टाइफून हार्डवेयर-इन-लूप (HIL).

Contents

Certificate	i
Acknowledgments	iii
Abstract	vi
Contents	viii
List of Figures	xii
List of Tables	xvi
Nomenclature	xvii
1 Introduction to Anti-islanding Protection	1
1.1 The Motivation of the Work	1
1.2 Existing Work and Research Gaps	3
1.2.1 Overview of Existing IDM	4
1.2.2 Non-Detection Zones of Islanding detection methods	5
1.2.3 Research Challenges in Existing Work	6
1.3 Thesis Objectives	8
1.4 Scopes and Common Assumptions	9
1.5 Brief Overview of Work Done	9

1.5.1	A New Event Triggered IDM Based on ROCOKE	10
1.5.2	The Analysis of Non-Detection Zones (NDZ) for Diverse Load Profiles . . .	10
1.5.3	The Impact of Islanding Detection Method on Power Quality	11
1.5.4	System Level Performance Analysis of The Proposed IDM	11
1.6	Thesis Outline	11
2	Event-Activated Hybrid Anti-Islanding Protection Framework	13
2.1	Introduction	13
2.2	System Overview and Inverter Control Strategy	14
2.2.1	Modified IEEE 1547 Test System	15
2.2.2	Calculation of RLC Parameters for a Perfectly Matched Loading Condi- tion	16
2.2.3	Classical Inverter Control	19
2.3	Proposed Islanding Detection Methodology	19
2.3.1	Kinetic Energy as triggering Parameter	21
2.3.2	Impact of Disturbance Current Injection in the Q-Axis of Inverter Control Loop	23
2.3.3	Proposed IDM Based on ROCOKE and RMS Frequency	27
2.3.4	Flowchart of the Proposed IDM	27
2.3.5	Parameter Setting of the IDM	29
2.4	Test Cases to Analyze the Proposed Methodology	30
2.4.1	Islanding Test Cases	31
2.4.2	Non Islanding Test Cases	32
2.5	Time Domain Analysis of the Proposed IDM	35
2.5.1	Performance of the Proposed Method During Various Islanding Events . .	36
2.5.2	Performance of the Proposed Method During Various Non-Islanding Events	38
2.6	Experimental Validation of Proposed IDM	41
2.6.1	Development Hardware Testing Setup	41

2.6.2	PHIL Testbed Used for the Experimental Validation	44
2.6.3	Real-time Performance Evaluation of Islanding Events	46
2.6.4	Real-time performance evaluation of non-islanding events	48
2.7	Conclusion	50
3	Impact of Load Variability on Non-Detection Zone (NDZ)	52
3.1	Introduction	52
3.2	Formulation of Power Balance Equation for NDZ Analysis	53
3.2.1	Power Balance Equation for Islanded Inverter	54
3.3	Effects of Load Variation on Non-Detection Zones (NDZ)	63
3.4	Case Study: Modeling of Real-Time EV Charging Load	65
3.4.1	System Description Under Case Study	65
3.4.2	EV Charging Data Processing	65
3.4.3	EV Charging Load Modeling with Curve Fitting	66
3.4.4	Mathematical Validation of Curve Fitting	67
3.5	The Influence of Different Load Models on Conventional Protection Schemes	69
3.5.1	Test System Under the Study	69
3.5.2	Parameter Setting	72
3.5.3	Time Domain Analysis	72
3.6	Conclusion	74
4	Power Quality Evaluation of Various Islanding Detection Methods	75
4.1	Introduction to Power Quality Issues in IDM	75
4.2	Impact of Parameter Variation on Voltage and Frequency of Inverter Output	76
4.2.1	System Description	77
4.2.2	Sandia Frequency Shift Method	80
4.2.3	Assessment of the Impact of Parameter Variations	82
4.3	THD Analysis Considering Parameter Variation	86

4.4	THD-Based Islanding Detection	87
4.4.1	System Description Used to Test the Proposed IDM	89
4.4.2	Control Architecture and Flowchart of the Proposed IDM	89
4.4.3	Time Domain Analysis	95
4.4.4	Results for Islanding Cases	95
4.4.5	Results for Non-islanding Cases	100
4.5	Hardware Validation of The Proposed THD-Based IDM	100
4.5.1	Experimental Testing Under Islanding Events	105
4.5.2	Experimental Testing Under Non-Islanding Events	108
4.6	NDZ of Proposed Method	108
4.7	Conclusion	113
5	System-Level Validation and Comparative Analysis of Active IDMs	114
5.1	Introduction	114
5.2	CIGRE LV Distribution Network a Real Word Microgrid Test System	115
5.2.1	System Description	115
5.3	Testing IDM under Various Test Cases on Real-World Systems	116
5.3.1	Performance Evaluation Under Islanding Events	118
5.3.2	Performance Evaluation Under Non-Islanding Events	119
5.4	Comparative Analysis of Different Active Methods of Islanding Detection	120
5.4.1	Various Parameters Considered for Comparison	122
5.5	Comparative Analysis of THD-based IDM and ROCOKE-based IDM	129
5.6	Conclusion	129
6	Conclusion and Future works	131
6.1	Conclusion	131
6.1.1	Promising Solutions: Novel Hybrid AIPS Methods	131
6.1.2	The Impact of Load Variability on The Non-detection Zone	132

6.1.3	IDM Parameter Setting and their Impact on Power Quality	132
6.1.4	System Level Validation of the Proposed Framework	133
6.1.5	Comparative Analysis of the Proposed Methodology	133
6.2	Future Work	134
6.2.1	Development of Adaptive IDM Algorithm	134
6.2.2	Extending Proposed Methodology for the Case of Grid Forming Inverters .	134
6.2.3	Integration of Multiple Microgrids and Analysis of the Proposed IDM in Various Operational Conditions	135
6.2.4	Collaboration with Industry Partners to Validate Proposed Methodologies .	135
6.2.5	Development of IDM Algorithm with the Additional Facilities to Differ- entiate between Islanding or Cyber Attack	135

List of Publications	144
-----------------------------	------------

Biodata	145
----------------	------------

List of Figures

1.1	Classification of Islanding Detection Methods	5
1.2	Existing work and Research gap	7
2.1	Schematic diagram of modified IEEE 1547 test system	15
2.2	Classical dq-axis Control loop	20
2.3	(a) Flow diagram for disturbance triggering (b) q-axis control with injected disturbance (c) Control loop for islanding detection	26
2.4	Flowchart of proposed method	28
2.5	Three phase voltage and current of inverter in an islanding event	35
2.6	Results for islanding event in perfectly matched condition	36
2.7	Results for islanding event unmatched condition	37
2.8	Results for islanding event with variation in load quality factor Q_f	37
2.9	Results for the islanding event when DG is not operating at unity power factor	38
2.10	Results for switching event	39
2.11	Results for phase jumping event	40
2.12	Results for load unbalancing event	41
2.13	Results for multiple non-islanding event occurrence	42
2.14	Hardware setup control block diagram	45
2.15	Hardware setup schematic representation	45

2.16	Real-time simulation results for islanding test cases (a) Perfectly Matched condition passive method (b) Perfectly Matched condition active method (c) Unmatched condition	47
2.17	The change in v_d and v_q before and after islanding conditions	48
2.18	Real-time simulation results non-islanding test cases (a) Switching event (b) Phase jump event	49
3.1	Power balance equations for RLC parallel load in anti-islanding test conditions . .	54
3.2	(a) NDZ sample space (b) NDZ for CIL model (c) NDZ for ZIP load model with (CPL=20 %, CCL= 20 % and CIL= 60 %) (d) NDZ for ZIP modeled EV load (e) NDZ comparison ((b), (c) and (d)) (f) NDZ for composite load model	64
3.3	Real-time setup for EV charging data collection	65
3.4	(a) Charging data, voltage, and corresponding power (b) State of charge concerning time (c) Curve fitting result for ZIP model (d) Curve fitting results for exponential load model	66
3.5	IEEE test system modified schematic design with EV charging load	70
3.6	Classical dq-axis control loop	71
3.7	Islanding event with constant power load and ZIP EV charging load	72
3.8	Impact of exponential EV charging load model on islanding	73
3.9	Impact of ZIP EV charging load model on islanding	74
4.1	Control blocks of classical dq-axis inverter control loop	78
4.2	Control blocks (a) Control loop with disturbance signal injected in q-axis (b) Control loop with disturbance signal injected in d-axis (c) SFS-based phase angle variation	79
4.3	Frequency drift method - operational waveform	81

4.4	Change in PCC voltage related to disturbance injection in d-axis (a) Disturbance signal Frequency change (b) Disturbance signal magnitude change (c) Loading condition at PCC change	83
4.5	Change in PCC frequency related to disturbance injection in q-axis (a) Disturbance signal Frequency change (b) Disturbance signal magnitude change (c) Loading condition at PCC change	84
4.6	Impact of SFS parameter variation on (a) frequency with change in K (b) voltage with change in k (c) frequency with change in cf_0 (d) voltage with change in cf_0 (e) on frequency with change in loading condition (f) voltage with change in loading condition	85
4.7	Power quality analysis (a) Sandia-phase angle variation (b) Disturbance injection in q-axis (c) Disturbance injection in d-axis	88
4.8	IEEE test system modified schematic design with EV charging load	90
4.9	Classical dq-axis control loop with proposed method	91
4.10	Control blocks for proposed AIPS based on THD measurements	92
4.11	Flowchart of proposed THD-based AIPS	93
4.12	Islanding events passive detection method	97
4.13	Islanding events active detection method perfectly matched loading case	97
4.14	Islanding events active detection method unmatched loading case	98
4.15	Impact of different sampling rate on Islanding Detection	99
4.16	Non-islanding events (a) DG output power change (b) Voltage fluctuations	101
4.17	Non-islanding events (a) Phase jump event (90°) (b) Unbalanced loading scenario	102
4.18	Non-islanding events (a) Switching of capacitor/inductor (b) High impedance fault	103
4.19	RTDS-Typhoon HIL 602+ PHIL testbed setup	104
4.20	Single line diagram of PHIL hardware connection (Test bed setup)	105
4.21	Power quality analysis (a) THD with and without disturbance signal (b) THD variations due to change in magnitude	106

4.22	Experimental results for various islanding test cases (a) Islanding in unmatched loading case (b) Islanding in perfectly matched loading scenario	107
4.23	Experimental results for various non-islanding test cases (a) Grid voltage change (b) Change in DG output power.	109
4.24	Experimental results for various non-islanding test cases (a) Unequal loading (b) Phase jump event.	110
4.25	Experimental results for various non-islanding test cases (a) High impedance fault near PCC (b) L/C switching event.	111
4.26	NDZ comparison of conventional technique with proposed method	112
5.1	Single line diagram of a modified CIGRE LV distribution network	117
5.2	Islanding event initiation at Bus-1 on the modified CIGRE LV distribution network	118
5.3	Islanding event initiation at Bus-4 on the modified CIGRE LV distribution network	119
5.4	Islanding event initiation at Bus-9 on the modified CIGRE LV distribution network	120
5.5	Non-islanding events Voltage fluctuations on the modified CIGRE LV distribution network	121
5.6	Non-islanding events Phase jump event on the modified CIGRE LV distribution network	121
5.7	Non-islanding events DG power change on the modified CIGRE LV distribution network	122

List of Tables

2.1	Parameters of the Test System	16
2.2	Various indices and their corresponding peak values.	21
2.3	Threshold Setting for IDM	29
2.4	Various Test Cases and Parameters Used	30
2.5	Various Standards and IDT	32
2.6	Hardware System Parameters and Values	44
3.1	Induction Motor Parameters	61
3.2	Various constant values	68
3.3	Parameters of the test system used to simulate the conventional IDM	70
4.1	Modified IEEE 1547 test system parameters	77
4.2	Comparative values voltage THD corresponding to parameter change	87
4.3	Parameters of the test system	90
4.4	Various test cases used for validation	96
5.1	Parameters of the modified CIGRE LV distribution network	116
5.2	Comparative study of different anti-islanding protection schemes	125
5.3	Comparative study of different anti-islanding protection schemes (Continued) . . .	126
5.4	Comparative analysis of proposed method with existing literature	128

Nomenclature

Acronyms/Abbreviations

SCADA Supervisory Control and Data Acquisition

AAIPS Adaptive Anti-Islanding Protection System

AC Alternating Current

AIPS Anti-Islanding Protection Scheme

C Capacitance

CCL Constant Current Load

CIGRE Conseil International des Grands Réseaux Electriques

CIGRE International Council on Large Electric Systems

CIL Constant Impedance Load

CIL Constant Impedance Load

CPL Constant Power Load

CV constant Voltage

DC Direct Current

DER	Distributed Energy Resources (DERs)
DG	Distributed Generators
DSO	Digital Storage Oscilloscope
EPDS	Electric Power Distribution System
EV	Electric Vehicle
f	Frequency
HIF	High Impedance Fault
HIL	Hardware in Loop
IBG	Inverter-Based Generation
IDM	Islanding Detection Methods
IDT	Islanding Detection Time
IEEE	Institute of Electrical and Electronics Engineers
IGBT	Insulated-gate Bipolar Transistor
IIS	Indian Interconnection Standards
IM	Induction Motor
IML	Induction Motor Load
KE	Kinetic Energy
L	Inductance
LV	Low Voltage

NDZ Non-Detection Zone

OF Over Frequency

OV Over Voltage

P Power

PCC Point of Common Coupling

PHIL Power Hardware in Loop

PI Proportional-Integral

PLL Phase-Locked Loop

PMU Phasor Measurement Units

PRBS Pseudorandom Binary Sequence

PWM Pulse Width Modulation

R Resistance

RLC Resistance-Inductance-Capacitance

RMS Root Mean Square

ROCOKE Rate of Change of Kinetic Energy

ROROKE Rate of Rise of Kinetic Energy

RSCAD Real-time Simulator Computer Aided Design

RTDS Real-Time Digital Simulator

SFS Sandia Frequency Shift

SOC	State of charge
SPS	Spitzenberger and Spies
THD	Total Harmonic Distortion
UF	Under Frequency
UL	Underwriters Laboratories
UV	Under Voltage
V	Voltage
VSC	Voltage Source Converter
ZIP	Constant Impedance, Constant Current and Constant Power