# C-2C LADDER BASED D/A CONVERTERS FOR PCM CODECS

By

S. P. SINGH

THESIS SUBMITTED
IN FULFILMENT OF THE REQUIREMENTS
OF THE DEGREE OF
**DOCTOR OF PHILOSOPHY**


Department of Electrical Engineering
INDIAN INSTITUTE OF TECHNOLOGY, DELHI
JUNE, 1986

## CERTIFICATE

This is to certify that the dissertation "C-2C ladder based D/A converters for PCM codecs" being submitted by S.P.Singh for the award of the degree of Doctor of Philosophy at the Indian Institute of Technology, Delhi, is a record of bonafide research work carried out by him under our supervision and guidance. In our opinion, it has reached the standard fulfilling the requirements of the regulation relating to the degree.

The results contained in this thesis have not been submitted to any other institute for the award of any degree or diploma.

**A. Prabhakar**
General Manager,
R & D, Indian Telephone
Industries Ltd.,
Bangalore 560 016

**A.B. Bhattacharyya**
Professor, Centre for Applied
Research in Electronics,
Indian Institute of Technology,
New Delhi-110 016

## ACKNOWLEDGEMENTS

I have great pleasure in expressing my gratitude to Dr.A.Prabhakar and Prof.A.B.Bhattacharyya for their supervision and guidance. Working with them has been a great experience.

I am grateful to Mr.B.S.Panwar for his invaluable support and help. I am also thankful to Dr.Sudhir Chandra, Dr.G.Bose, and Mr.Rajinder Singh for their help and suggestions.

I express my sincere thanks to Mr.G.H.Sarma for the encouragement during the course of work. I am also grateful to Mr.P.V.S.Subramanyam, Dr.(Mrs.)N.Menon, Mr.D.Sarkar, Dr.V.Kalyanaraman, Mrs.M.Sarkar, Mr.S.Annamalai, Dr.(Mrs.) S.Sen, Dr.C.Rajagopal, Mr.G.Viswanadam, Mr.H.L.Pratap, Mr.C.N.Ajit, and Mr.B.S.Chandrashekar for their help in the fabrication and testing of the chip.

I also thank the Management of Indian Telephone Industries Limited, Bangalore-560 016, for their permission and support during the course of this work.

I thank Mr.J.Natarajan and Mr.L.Balakrishna for the help in entering and editing the text on the word processor.

My thanks are also due to my wife and kids who showed a great amount of patience and restraint.

S.P.SINGH

## ABSTRACT

D/A and A/D converters based on the binary weighted capacitor array, and various derivatives thereof, have been extensively studied in the literature. PCM voice codecs incorporating such converters are available as standard commercial products. This thesis is devoted to the analysis, design and simulation of C-2C ladder-based D/A converters, which do not appear to have been studied so far in the literature.

It is shown first, that the capacitor bottom plate parasitics result in unacceptably high ($> 0.5$ LSB) nonlinearity of C-2C ladder D/A converters. Therefore, it is suggested that these parasitics should be "designed in", i.e., be treated as circuit elements rather than as parasitics, and incorporated into the converter design. To this end, a unit capacitor C is proposed, which has a linear floating bottom plate parasitic $C_p$.

Two design approaches are developed, one based on the assumption that $C_p \ll C$ and the other assuming $C_p/C \simeq 10\%$, culminating in 7-bit designs with nonlinearity as low as 0.095LSB. These 7-bit designs are then extended to 13 bits. A series of 13-bit designs are obtained, the most economical of which has a unit capacitor count as low as 39 -- a drastic reduction over the best reported so far in the literature, i.e., 192.

Finally, guidelines are developed for converter mask layout design, and it is experimentally verified that the procedure of designing in the parasitics does indeed drastically reduce converter nonlinearity.

# CONTENTS