CONTROLLING OF PV INTEGRATED GRID-TIED CONVERTERS: REDUCED DC-LINK CAPACITOR AND REDUCED SENSORS

KHUSHBOO KUMARI

DEPARTMENT OF ELECTRICAL ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY DELHI
FEBRUARY 2024

CONTROLLING OF PV INTEGRATED GRID-TIED CONVERTERS: REDUCED DC-LINK CAPACITOR AND REDUCED SENSORS

A THESIS

submitted by

KHUSHBOO KUMARI

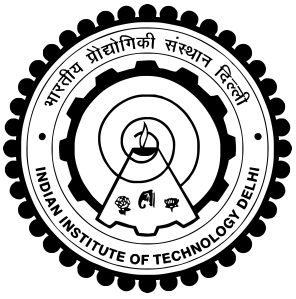
under the supervision of

Prof. Amit Kumar Jain

in fulfillment of the requirements of the degree

of

Doctor of Philosophy



Department of Electrical Engineering
INDIAN INSTITUTE OF TECHNOLOGY DELHI

FEBRUARY 2024

Certificate

This is to certify that the thesis titled **"CONTROLLING OF PV INTEGRATED GRID-TIED CONVERTERS: REDUCED DC-LINK CAPACITOR AND REDUCED SENSORS"**, submitted by **Khushboo Kumari**, for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, Indian Institute of Technology, Delhi, is a bonafide record of the research work done by her under my supervision. The contents of this thesis, in full or in parts, have not been submitted to any other Institute or University for the award of any degree or diploma.

Dated:

(Dr. Amit Kumar Jain)
Department of Electrical Engineering
Indian Institute of Technology, Delhi
Hauz khas, New Delhi-110016, India

Acknowledgements

It is my pleasure to remind and acknowledge the outstanding individuals, who in one way or another provided stupendous support in the completion of my doctoral research. This thesis would not have been possible without the guidance and assistance of such extraordinary persons.

First of all, I would like to express my special thanks of gratitude to **Prof. Amit Kumar Jain**, my thesis supervisor, for continuous support and for taking me through thick and thin during the course of my research journey. I always admire his patience and calm stature. His insight and discernment have led me to get the maximum in my research area. The consequence of persistent brainstorming sessions with him has yielded several ideas that have helped me to complete my research work. He is truly an extraordinary advisor who has extended his help in my doctoral research and offered significant support in balancing my professional and personal life.

Second, I would like to thank my review committee members, **Prof. M. Veerachary**, **Dr. Anandarup Das**, and **Dr. Ashu Verma**, for constantly supervising, providing suggestions, and thoughtfulness through research progress sessions which have led me to improvise and refine my research work. I would like to thank **Prof. Amit Kumar Jain** and **Dr. Anandarup Das** for providing an excellent research environment and laboratory facilities. I also like to thank **Mr. Sumit Kumar Singh**, **Mr. Dhanraj Singh**, and late **Mr. Suresh Chand** for assisting in procuring items for the experimental setup.

I would also like to express my sincere thanks to my seniors, peers, and colleagues for constantly getting involved in technical discussions. I would like to especially thank **Miss Cheshta Jain** for supporting me emotionally and spiritually during tough times. I would also like to acknowledge the efforts of my seniors **Dr. Prasun Mishra**, **Dr. Kapil Shukla**, and **Dr. Nikhil Krishna Bajjuri** to uplift my motivation and encourage me while implementing my experimental setup. I will always cherish **Mr. Navneet Vaishnav** for having technical discussions on the control aspect. I would also like to thank **Mr. Rahul Sharma** and **Mrs. Nidhi Bist** for constantly helping me in my personal as well as professional life. I would also send my best wishes and thanks to all the lab-mates, **Mr. Martin Cheerangal**, **Mr. Aamir Rafiq**, and **Miss Apurva Verma**.

Lastly, I revere my parents and all my family members for constantly motivating, encouraging, and supporting me through my research journey. Especially, I would like to express my sincere gratitude to my husband for being patient and calm during the course of my research work.

(Khushboo Kumari)

Abstract

This thesis deals with the analysis, modeling, simulation, and implementation of solar photovoltaic (PV) integrated grid-tied neutral point clamped (NPC) converters. The converter is interfaced with the grid through an *LCL* filter, which introduces resonance in the grid current. The resonance in the grid current leads to instability in the system. This thesis contributes to the control aspect, minimization of complexity, and increases reliability and harmonic content in the implementation.

Extensive loss analysis is carried out between NPC and T-Type three-level converter for different semiconductor devices based on Si, SiC, and GaN comprehensively. This facilitates the selection of the best three-level converter for the grid-tied converter. The three-level NPC is chosen for interfacing solar PV to the grid. To meet the demand for reduction in cost and weight and also increase in reliability of the *LCL* filter-based grid-tied converter, a cascaded control for the *LCL* filter-based grid-connected NPC inverter with the reduced sensor is proposed and incorporated in the thesis. Multiple loop control strategies are generally preferred to achieve better system stability. However, the multiple loop control technique utilizes numerous sensors, which increases weight, and cost and decreases the system's reliability. A novel cascaded control scheme that considerably reduces grid-side current and capacitor-side voltage sensors is implemented. Only two inverter-side current sensors are required. The proposed estimation algorithm implements the sensing point. Estimating the grid-side current and the capacitor voltage is carried out through the sensed inverter side current. Another less sensor-based scheme is proposed in this thesis that is based on sensing capacitor side voltage for the *LCL* filter-based grid-connected NPC inverter.

The robust and stable control technique utilizing less number of sensors is a significant concern in *LCL* filter-based grid-connected converter for the weak grid that requires considerable research attention. This thesis incorporates a Trilateral control scheme for *LCL* filter-based system with a single grid current sensor in the weak grid. This work implements a novel control scheme utilizing a single sensor to sense the grid current. This technique has reduced a considerable number of current sensors and voltage sensors. The α axis of the grid current is proportional to the sensed 'a' phase grid current. The β current in the utility grid is acquired by employing the controller reference quantities of the grid current. The computation of another variable, *i.e.,* the current in the inverter side inductor and the voltage across the capacitor, is executed by an estimation algorithm. The proposed technique provides the feature of reducing implementation financial value and weight and reduces the complexity and size of hardware.

In order to enhance the reliability, lifetime expectancy, improved efficiency, and reduced cost of the system, an effective reduction in the capacitor size of the DC-bus of a conventional three-phase NPC inverter-based grid-integrated single-stage solar photovoltaic (PV) system is also integrated into the thesis. It also retains the feature of minimal oscillations during the change in irradiation.

A twelve insulated gate bipolar transistor (K40H603) with their appropriate drivers and six diodes (FFPF30UA60S) based experimental set-up is developed in the laboratory. Texas instruments-based DSP TMS320F28335 digital controller is utilized to run the set-up. The system performance is observed using a MATLAB version simulation model and authenticated through the experimental results obtained from the laboratory prototype.

सारांश

यह थीसिस सौर फोटोवॉल्टेक (PV) इंटीग्रेटेड ग्रिड–टाइड न्यूट्रल पॉइंट क्लैम्प्ड (NPC) कनवर्टर्स के विश्लेषण, मॉडलिंग, सिमुलेशन, और अमलीकरण के साथ संबंधित है। कनवर्टर ग्रिड से LCL फिल्टर के माध्यम से इंटरफेस्ड है, जो ग्रिड के वर्तमान में रीसोनेंस लाता है। ग्रिड के वर्तमान में रीसोनेंस सिस्टम में अस्थिरता की ओर ले जाता है। यह थीसिस नियंत्रण पहलू, जटिलता की कमी, और अमलीकरण में सत्ता और हार्मोनिक सामग्री को कम करने में योगदान करती है।

एनपीसी और टी–टाइप तीन स्तरीय कनवर्टर के बीच व्यापक हानि विश्लेषण प्रदर्शित किया गया है जो विभिन्न सिलिकॉन, एसआईसी, और गैन पर आधारित अलग–अलग अर्धचालक उपकरणों के लिए होता है। यह सूर्य PV को ग्रिड से इंटरफेस करने के लिए तीन स्तरीय एनपीसी का चयन करता है। लागत और वजन में कमी और सुरक्षा में वृद्धि के लिए एलसीएल फिल्टर आधारित ग्रिड–टाइड कनवर्टर के लिए एक कास्केड नियंत्रण प्रस्तावित किया गया है और थीसिस में शामिल किया गया है। मल्टीपल लूप नियंत्रण रणनीतियों को सामान्यतः बेहतर सिस्टम स्थिरता प्राप्त करने के लिए पसंद किया जाता है। हालांकि, मल्टीपल लूप नियंत्रण तकनीक कई सेंसरों का उपयोग करती है, जो वजन और लागत बढ़ाता है और सिस्टम की सुरक्षा को कम करता है। एक नवीन कास्केड नियंत्रण योजना जो ग्रिड साइड करंट और कैपेसिटर साइड वोल्टेज सेंसर को कम करने के लिए काफी अच्छा है, प्रस्तावित किया जाता है। केवल दो इन्वर्टर–साइड करंट सेंसर की आवश्यकता है। प्रस्तावित अनुमान एल्गोरिदम सेंसिंग प्वाइंट को लागू करता है। ग्रिड–साइड करंट और कैपेसिटर वोल्टेज का अनुमान इंवर्टर साइड करंट के माध्यम से किया जाता है। एक और कम सेंसर–आधारित योजना को इस थीसिस में प्रस्तावित किया गया है जो LCL फिल्टर आधारित ग्रिड–टाइड NPC इन्वर्टर के लिए कैपेसिटर साइड वोल्टेज

सुदृढ़ और स्थिर नियंत्रण तकनीक जो कम संख्या में सेंसर का उपयोग करती है, वे दुर्बल ग्रिड के लिए LCL फ़िल्टर आधारित ग्रिड–कनेक्टेड कनवर्टर में महत्वपूर्ण चिंता है जो विशेष रूप से अध्ययन की जरुरत है। यह थीसिस LCL फ़िल्टर आधारित प्रणाली के लिए एक त्रिकोणीय नियंत्रण योजना को शामिल करती है जिसमें एक ही ग्रिड करंट सेंसर का उपयोग दुर्बल ग्रिड में किया जाता है। यह काम ग्रिड करंट को महसूस करने के लिए एक ही सेंसर का उपयोग करने वाली एक नई नियंत्रण योजना को लागू करता है। इस तकनीक ने एक बड़ी संख्या की सेंसर और वोल्टेज सेंसर को कम किया है। ग्रिड करंट का α धुरी जो 'a' चरण ग्रिड करंट को महसूस करने के लिए है, यह β करंट उपयोग करता है जो सेंसर करंट कंट्रोलर संदर्भ मात्राओं का उपयोग करके उपयोगिता ग्रिड में है। एक अन्य परिवर्तन, अर्थात इनवर्टर साइड इंडक्टर में करंट और कैपेसिटर के वोल्टेज की गणना एक अनुमान एल्गोरिथम के द्वारा की जाती है। प्रस्तावित तकनीक को अमलीकरण वित्तीय मूल्य और वजन को कम करने की सुविधा प्रदान करती है और हार्डवेयर की जटिलता और आकार को कम करती है।

सिस्टम की विश्वसनीयता, जीवनकाल अपेक्षा, बेहतर कुशलता, और कम लागत को बढ़ावा देने के लिए, एक पारंपरिक तीन–चरण NPC इन्वर्टर आधारित ग्रिड–इंटीग्रेटेड एक–मंजिल सौर फोटोवोल्टेक (PV) सिस्टम के DC–बस के कैपेसिटर के आकार में प्रभावी कमी भी थीसिस में शामिल की गई है। यह भी इसकी विशेषता को बनाए रखता है कि प्रकाश संचार में परिवर्तन के दौरान न्यूनतम अदल–बदल होता है।

एक बारह इंसुलेटेड गेट बायपॉलर ट्रांजिस्टर (K40H603) के साथ उनके उपयुक्त ड्राइवर और छह डायोड (FFPF30UA60S) पर आधारित प्रयोगशाला सेट–अप विकसित किया गया है। टेक्सास इंस्ट्रूमेंट्स आधारित DSP TMS320F28335 डिजिटल नियंत्रक का उपयोग सेट–अप को चलाने के लिए किया गया है। सिस्टम के प्रदर्शन को एक MATLAB संस्करण सिमुलेशन मॉडल का उपयोग करके देखा गया है और प्रयोगशाला प्रोटोटाइप से प्राप्त प्रयोगात्मक परिणामों के माध्यम से प्रमाणित किया गया है।

Contents

List of Figures

List of Tables

Abbreviations

AC	Alternating Current
ANF	Adaptive Notch Filter
CDF	Cumulative Density Function
CHB	Cascaded H-Bridge
DC	Direct Current
DSOGI	Dual Second Order Generalized Integrator
DSP	Digital Signal Processor
EA-P&O	Enhanced Adaptive Perturb and Observation
EPLL	Enhanced Phase-Locked Loop
ESR	Equivalent Series Resistance
FFT	Fast Fourier Transform
GaN	Gallium Nitride
GPIO	General Purpose Input Output
IGBT	Insulated-gate bipolar transistor
IIR	Infinite Impulse Response
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LF	Loop Filter
LPF	Low Pass Filter
M&R	Maintenance and Repair
M-DSOGI	Modified Dual Second Order Generalized Integrator
MNF-SOGI	Modified Notch Filter based Second-Order Generalized Integrator
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MPPT	Maximum Power Point Tracking
MTTR	Mean Repair Time of the System
NF	Nyquist Frequency
NPC	Neutral Point Clamped Converter
OLTF	Open Loop Transfer Function
P&O	Perturb and Observe
PBC	Passivity-based Control
PCC	Point of Common Coupling
PD	Phase Detector
PLL	Phase Locked Loop
PV	Photo Voltaic

PWM	Pulse Width Modulation
RF	Resonant Frequency
RMS	Root Mean Square
Si	Silicon
SiC	Silicon Carbide
SOGI	Second Order Generalized Integrator
SPWM	Sinusoidal Pulse Width Modulation
SRF	Synchronous Reference Frame
SRF-PLL	Synchronous Reference Frame Phase Locked Loop
TF	Transfer Function
THD	Total Harmonic Distortion
TLC	Three Loop Control
UPS	Uninterrupted Power Supply
VCO	Voltage-Controlled Oscillator
VFI	Voltage-Fed Inverter
VSI	Voltage Source Inverter

Nomenclature

ω_c, ω_r	$2\pi f_c, 2\pi f_r$
C	LCL filter capacitance
C_b	BaseLCL filter capacitance
C_{dc}	DC-link capacitance
C_{part}, C_{lt}	Replaced part cost and labor, including travel cost
$d_+ - q_+$	Positive d-q synchronous reference frame
$d_- - q_-$	Negative d-q synchronous reference frame
f_b	Bandwidth
f_g	Grid frequency
f_s, f_{sw}, T_s	Sampling frequency, switching frequency, sampling time
f_r, f_c	Resonance frequency, cut off frequency
f_{res}	Resonant frequency
$F(x)$	Weibull distribution's CDF
G_m, P_m	Gain margin, phase margin
i_{gde}, i_{gqe}	Estimated grid current in d and q axis
i_{ga}, i_{gb}, i_{gc}	Grid currents
i_{gd}, i_{gq}	Grid currents in d and q axis
$i_{gd*}, i_{gde}, i_{gq*}, i_{gqe}$	Reference and estimated grid currents in d and q axis
i_{gm}, v_{cm}, i_{im}	Measured grid current, capacitor voltage, and inverter current
i_{gdm}, i_{gqm}	Measured grid current in d and q axis
$i_{g\beta e}$	Estimated grid's current in a β axis
i_{ia}, i_{ib}, i_{ic}	Inverter currents
$i_{id*}, i_{id}, i_{iq*}, i_{iq}$	Reference and measured inverter currents in d and q axis
i_{ide}, i_{iqe}	Estimated grid currents in d and q axis
$I_N, I_{c,rms}$	Grid phase current and rms of the DC-bus capacitor ripple current
k	Variable used for neutral point voltage controller
k_{max}, k_{min}	Reference signal for the upper carrier, and the lower carrier
k_{p1}, k_{i1}	PI of outer loop
k_{p2}, k_{i2}	PI of middle loop
k_{p3}, k_{i3}	PI of inner loop
L_{equ}, α	Equivalent inductance $L_1 + L_2$, $\frac{L_2}{L_1}$
L_{gmin}, L_{gmax}	Grid inductance minimum and maximum value
L_x, L_r	Time to failure in hour and time to failure at the rated voltage in hour
N_c, N	Number of components and number of years
PI_1, PI_2, PI_3	Outermost loop, middle loop, and innermost loop
P_r, P_D, P	The rated active power, power dissipation, and inverter output power
R_1, L_1	Inverter side resistance and inductance of LCL filter
R_2, L_2	Grid side resistance and inductance of LCL filter
R_g, L_g	Grid resistance and inductance
T_d	Delay time

T_a, T_h	Ambient temperature and hot spot temperature
v_{ao}, v_{bo}, v_{co}	Inverter terminal voltages
v_a, v_b, v_c	Phase inverter voltages
v_{ab}, v_{bc}, v_{ca}	Line to line inverter voltages
v_{cde}, v_{cqe}	Estimated capacitor voltage in d and q axis
$v_{cd*}, v_{cde}, v_{cq*}, v_{cqe}$	Reference and estimated capacitor voltages in d and q axis
v_{cdm}, v_{cqm}	Measured filter capacitor voltages in d and q axis
v_c, V_{gl-l}	Capacitor voltage and line-to-line grid voltage
v_{ca}, v_{cb}, v_{cc}	Capacitor voltages
v_{cd}, v_{cq}	Capacitor voltages in d and q axis
$v_{c(d_e)}, v_{c(q_e)}$	Estimated capacitor voltages in d and q axis
v_{dc1}, v_{dc2}	DC-link voltage across capacitors
v_{dc}	DC-link voltage
v_g, i_g	Grid voltage and grid current
v_{ga}, v_{gb}, v_{gc}	Grid voltages
v_i, i_i	Inverter voltage and grid current
v_{ia}, v_{ib}, v_{ic}	Inverter voltages
v_{id}, v_{iq}	Inverter output voltage in d and q axis
V_{out}, I_{out}	Inverter output voltage and current
$v_{pcca}, v_{pccb}, v_{pccc}$	Point of common coupling voltages in phase a,b,and c
v_{pccd}, v_{pccq}	Point of common coupling voltages in d and q axis
v_{pv}, i_{pv}, P_{pv}	PV voltage, current, and power
v_r, v_x, V_{ripple}	Rated voltage, used voltage, and ripple voltage
I_r, I_x	Ripple current, and applied ripple current
z_b, ϕ	Base impedance
ϕ	Phase delay of the grid current w.r.t the fundamental grid voltage