

**A NEW AUGMENTED DATA VORTEX
ALL OPTICAL INTERCONNECTION NETWORK
WITH
PERFORMANCE EVALUATION AND
FAULT TOLERANCE STUDIES**

BY

NEHA SHARMA (nee TRIPATHI)
Department of Electrical Engineering

Submitted
In fulfillment of the requirements of the degree of
DOCTOR OF PHILOSOPHY

to the



**INDIAN INSTITUTE OF TECHNOLOGY, DELHI
INDIA**

February 2008

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CERTIFICATE

This is to certify that the thesis entitled “**A New Augmented Data Vortex All Optical Interconnection Network with Performance Evaluation and Fault Tolerance Studies**” being submitted by Neha Sharma to the Department of Electrical Engineering, Indian Institute of Technology, Delhi, for the award of degree of Doctor of Philosophy is the record of the bona-fide research work carried out by her. She has worked under our supervision and guidance. The thesis, in our opinion has reached the standards fulfilling the requirements of the regulations relating to the degree. The results contained in this thesis have not been submitted either in part or in full to any other university or institute for the award of any degree or diploma.



Professor D. Chadha

Department of Electrical Engineering
Indian Institute of Technology, Delhi
New Delhi - 110016



Professor Vinod Chandra

Department of Electrical Engineering
Indian Institute of Technology, Delhi
New Delhi - 110016

ACKNOWLEDGEMENTS

“Gratitude is the hardest of emotion and often does not find adequate words to convey that entire one feels.” I feel the same when I express my profound gratitude to my Ph. D. supervisors Prof. D. Chadha and Prof. Vinod Chandra for their invaluable guidance and continuous encouragement during the entire period of this research work. Their technical acumen, precise suggestions and timely discussions, whenever I was in some problem, is wholeheartedly appreciated. Through their extremely humble, simple, and considerate nature, I could pursue my research work inspite of many hindrances. They have devoted a lot of time in formulating the research problem, and analyzing and discussing the results. They were ever so patient to the wall of ignorance that I so often presented. With all my respect I indeed extend heartfelt gratitude to them.

I am also thankful to my Student Research Committee members Prof. B. P. Pal and Prof. S. Kar, Dr. S. Prakriya, for providing their critical comments and constructive suggestions.

I wish to express my thanks to the Technical Education Department of Government of Madhya Pradesh for deputing me under Quality Improvement Programme (QIP) to carry out this research work. Thanks are also due to Prof. S. R. Nigam, Principal, Government Engineering College, Sagar (M. P.) for allowing me to continue with my Ph.D. work in spite of heavy workload. I would also like to thank the faculty members and other staff of I. G. Government Engineering College, Sagar, (M.P.) for being so cooperative.

I will always fall short of words in expressing my gratitude to my parents. They have nurtured me and my aspirations with sublime care. What I am today I owe it all to them.


I also owe my heartfelt gratitude for my parents-in-law who were always so understanding and cooperative. I gratefully acknowledge both of my sisters, Gayatri and Annapurna, and their husbands Mr. Vinay and Mr. Alok respectively, for constant encouragement and help to keep my enthusiasm high throughout the duration of this work. I owe my sincere thanks to all my relatives and friends who have always encouraged me during my research work. I would specially like to thank Mrs. Shanta K. Chandra, w/o Prof. Chandra for the moral support provided by her throughout this

period. There are several others with whom I have shared priceless moments. They go unmentioned for want of space, but I would like to express my sincere thanks to them.

I would like to thank Ms. Neeru Asija, Mr. A. P. Thakral, Mr. J. P. Naudiyal, and Mr. G. S. Negi for the helpful atmosphere and cooperation they have extended to me in Optics Lab. I also wish to thank Indian Institute of Technology in general, and Electrical Engineering Department in particular, for providing me an opportunity to pursue my Ph.D. in its wonderful academic environment. I feel myself to be fortunate one to be a part of this premiere institution, IIT Delhi.

Finally, I express my sincere and hearty feelings to my husband, Pradeep, for his moral and emotional support throughout the period of research work. Last, but not the least, I thank my children, Shivam and Manu who had to miss number of affectionate hours that truly belonged to them during the course of this work.

Date: 27.2.2008


(NEHA SHARMA (nee TRIPATHI))

ABSTRACT

In this thesis we have proposed a new *Augmented Data Vortex (ADV) switch*, an all optical packet switched interconnection network. The ADV proposes to (i) improve the fault tolerance of the all optical Data Vortex (DV) packet switch, which is reported as the more recent all optical packet switch that overcomes the limitations of optical buffering using fiber delay lines, optical bit level processing, TDM header and payload synchronization in optical domain, and also enjoys the features of high capacity, low latency, high scalability, low cross talk; and (ii) reduce the overall latency within the network, without degrading the performance regarding throughput and scalability.

The thesis is concerned with the topological, fault tolerance and performance related issues of the ADV network. The new interconnections, self routing, distributed control signaling, and optical domain implementation of the switch have been suggested. Results of fault tolerance and reliability in ADV have been evaluated through analytical study. Closed form expressions for fault tolerance, reliability, and all possible paths in ADV have been obtained. Performance regarding latency, latency distribution, and throughput, has been evaluated through numerical simulations. To assure performance and reliability in ADV, and to know the degradation in latency due to occurrence of faults, we have also evaluated the latency performance of the ADV under worst faulty condition. Also, the equivalent planar model for the 3 dimensional ADV and DV switches have been found which are more suited for topological comparisons with other multi stage interconnection networks.

The results obtained for ADV network have been compared with the DV switch.

CONTENTS

	Page no.
1. INTRODUCTION	
1.1 General	1
1.2 Literature Survey	3
1.2.1 Interconnection networks	3
1.2.2 The Data Vortex switch	6
1.3 Motivation of Present Work	8
1.4 Organization of the Thesis	9
2. THE AUGMENTED DATA VORTEX NETWORK	
2.1 Introduction	12
2.2 Labeling, numbering, interconnection of nodes, distributed control signaling, and implementation issues in ADV switch	14
2.2.1 Labeling and numbering scheme	15
2.2.2 Interconnection of nodes	16
2.2.3 Distributed control signaling in ADV switch	16
2.3 Equivalent planar chained-MIN model for the 3-dimensional ADV switch with multiplexing at input and output terminals	20
2.3.1 Equivalent planar model	20
2.3.2 Multiplexing of input and output terminals for improved fault tolerance	22
2.4 Self-routing scheme for the ADV switch	22
2.5 Conclusions and discussions	24
3 FAULT TOLERANCE AND RELIABILITY EVALUATION IN AUGMENTED DATA VORTEX NETWORK	
3.1 Introduction	26
3.2 Fault tolerance evaluation in ADV	27
3.2.1 Fault model	27
3.2.2 Deterministic and random approaches	29
3.2.3 Upper bound on the number of tolerable faulty elements in	

	ADV switch	29
	3.2.4 Expected number of tolerable faults in the ADV switch	31
3.3	Fault tolerance evaluation in DV	36
	3.3.1 The Multiplexed DV network and its equivalent planar MIN Model	37
	3.3.2 Fault tolerance evaluation	37
3.4	Network reliability	41
	3.4.1 Mean time to failure (MTTF) of the ADV switch	42
	3.4.2 Mean time to failure (MTTF) of the DV switch	43
3.5	Terminal Pair Reliability	44
	3.5.1 Matrices for Connections of an Interconnection Network	44
	3.5.2 Modified Matrices for ADV Network	45
	3.5.3 All Possible Paths for the ADV Network	47
	3.5.4 Reliability Evaluation of the ADV Network	54
	3.5.5 Reliability Comparison with the DV Network	55
3.6	Hardware complexity and cost effectiveness	57
3.7	Results: Fault tolerance, reliability, hardware complexity and cost effectiveness	58
3.8	Conclusions and discussions	60
4	PERFORMANCE EVALUATION OF AUGMENTED DATA VORTEX NETWORK	
4.1	Introduction	62
4.2	Simulation Method	62
4.3	Simulation results	66
	4.3.1 Latency	66
	4.3.2 Latency Distribution	68
	4.3.3 Injection rate	70
4.4	Conclusions and discussions	72

5	LATENCY EVALUATION OF AUGMENTED DATA VORTEX NETWORK UNDER FAULTY CONDITION	
5.1	Introduction	74
5.2	Latency evaluation in ADV– An example	75
	5.2.1 Setup and procedure for latency evaluation	75
5.3	Latency evaluation in non faulty ADV	77
	5.3.1 Results for non faulty ADV	79
5.4	Latency evaluation in worst case faulty ADV	80
	5.4.1 Fault model	80
	5.4.2 Creating worst case faulty ADV	80
	5.4.3 Latency evaluation	83
	5.4.4 Results for worst case faulty ADV	83
5.5	Conclusions and discussions	84
6	CONCLUSIONS AND SCOPE FOR FUTURE WORK	
6.1	Summary of contributions	85
6.2	Scope for future work	
	6.2.1 Limitations	87
	6.2.2 Possible approaches	88
	REFERENCES	89