

A MULTI-LEVEL ASSOCIATIVE PROCESSOR ARCHITECTURE  
FOR PARALLEL PROCESSING

BY  
SHASHI KUMAR

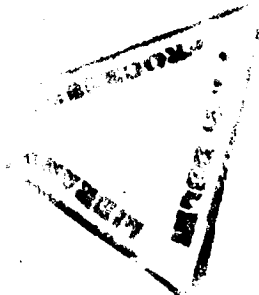
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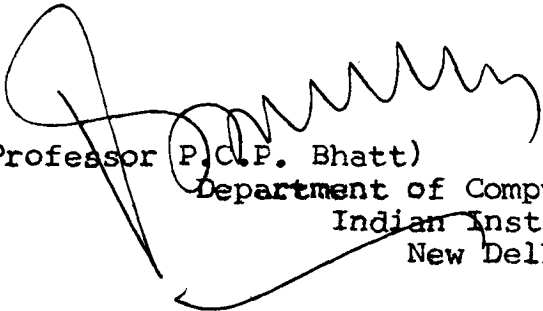
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C E R T I F I C A T E

This is to certify that the thesis entitled, "A Multi-Level Associative Processor Architecture for Parallel Processing", being submitted by Shashi Kumar to the Indian Institute of Technology, Delhi for the award of the degree of Doctor of Philosophy, is a record of bonafide research work carried out under our supervision. The results contained in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

  
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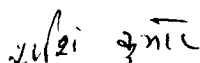
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- Shashi Kumar

## A B S T R A C T

In this thesis a high performance parallel processing computer architecture, called Multilevel Associative Processor (MLAP) architecture, is proposed. A MLAP consists of a tree of associative memory cells. All the direct descendants of a cell in the cell tree are interconnected through a mesh network. The architecture provides coordinate addressing by which a subset of direct descendants can be selected for parallel processing. It is shown that a MLAP can solve many problems more efficiently than a Conventional Associative Processor. If the data is assumed to be already available in a MLAP, then it can multiply two  $N \times N$  matrices in  $O(W^2 \log N)$  time and sort a list of  $N$  numbers in  $O(W \log N)$  time, where  $W$  is the number of bits of the involved operands. It is also shown that all relational data base primitive operations have efficient implementations on MLAP, if the entire relations are stored in MLAP. Two layouts for VLSI implementation of MLAP are proposed and their areas are worked out using Thompson's VLSI model. Based upon the area calculations and technology predictions, a set of feasible VLSI chips are proposed for the proposed architecture. A Data Base Machine design around a MLAP using a head/track mass storage device is also described. Data Base operations involving **single** relation takes time independent of the cardinality of the involved relation on the proposed machine. Join takes time proportional to the cardinality of the resultant relation. The analysis is based upon uniform random distribution of tuples

of the involved relations, on the disk. Parallelization of multi-nested loops for MLAP is also discussed. It is shown that on a 3-Level AP ~~all~~ multinested loops, except for the subset of loops in which the execution of the loop body for an iteration depends upon a variable modified by an earlier iteration, can be executed simultaneously for all combinations of indices.

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