A FEW ASPECTS IN THE PERFORMANCE OPTIMIZATION OF SURFACE CHANNEL CHARGE COUPLED DEVICES IN ANALOG SIGNAL PROCESSING

A thesis
submitted for the degree of
DOCTOR OF PHILOSOPHY
in Electrical Engineering

By
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to the

INDIAN INSTITUTE OF TECHNOLOGY, DELHI
November 1983

CERTIFICATE

This is to certify that the dissertation "A few aspects in the performance optimization of surface channel charge coupled devices in analog signal processing" being submitted by L. Sankara Narayanan for the award of the degree of Doctor of Philosophy at the Indian Institute of Technology, Delhi, is a record of bonafide research work carried out by him under our supervision and guidance. In our opinion, it has reached the standard fulfilling the requirements of the regulation relating to the degree.

The results contained in this thesis have not been submitted to any other institute for the award of any degree or diploma.

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ACKNOWLEDGEMENTS

I acknowledge with pleasure the encouragement and guidance of Professor A.B. Bhattacharyya and Professor S.C. Dutta Roy. I am grateful to them for introducing me to the fascinating field of CCD technology and application.

I am thankful to Dr. J. Vasi, Dr. Bimal Mathur and Dr. D. Nagchoudhry for their helpful suggestions during this study. My thanks are due to Dr. U.K. Chakrabarti, Dr. Navin Kapur, Dr. Sudhir Chandra, Dr. S.K. Madan and other members of Solid State Device group for their suggestions and support during this work.

I gratefully acknowledge the financial support extended by Indian Institute of Technology, Delhi, and Department of Electronics, Government of India, during the course of this research work.

I am also thankful to Mr. J. Holleman, Twente University of Technology, The Netherlands, for the fabrication of the poly-Si gate CCDs.

I am thankful to Mr. V.N. Sharma for typing the thesis, and to Mr. Kapoor for drafting the figures. I am also thankful to Mr. Amar Singh for cyclostyling the thesis.

I am grateful to my parents, but for whose moral support and encouragement, this work would not have been possible.

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ABSTRACT

This thesis deals with the optimization of the performance of surface channel charge coupled devices (SCCDs) by optimizing the driving conditions of the device. Minimization of the charge backflow loss which is dependent on the clocking scheme, and maximization of the bandwidth and dynamic range of the CCD are dealt with in detail. A linearized small signal expression for the dispersion introduced due to charge backflow loss is derived. A new technique of characterization of the backflow loss and incomplete forward transfer loss is developed. The effect of truncated feedback compensation (which compensates for the dispersion introduced due to transfer inefficiency) on the dynamic range of the CCD, is studied. It is established that for compensating the effect of charge backflow related transfer inefficiency, a significant sacrifice in the dynamic range is required. However, it is shown possible to minimize backflow loss without incurring a reduction in the dynamic range, by optimizing the driving clock waveform. An extensive analysis of the free charge transfer in surface channel, three phase CCDs is carried out so as to determine the influence of clock waveform on the performance of the device and to find the optimum clocking conditions. A modified three level clocking operation is suggested which is shown to help in overcoming the limitations introduced by charge backflow phenomenon on the high frequency charge transfer efficiency and dynamic range of the CCD.

The clocking conditions required for optimizing the performance of floating gate tapped CCDs (which have applications in transversal filtering) are also studied. A virtual two phase clock waveform having a critical dc off-set between the two driving clocks is shown to be advantageous for enhancing the charge handling capability of floating sense gates. Further, the dc off-set helps to minimize the clock turn-off time thereby enhancing the charge transfer speed or the high frequency charge transfer efficiency. The critical requirements of the dc off-set and the turn-off time of the clocks for optimal operation of a floating gate tapped CCD programmable transversal filter are discussed. The advantages and disadvantages of using a novel area variable MOS capacitance weighting technique for realizing the programmable tap-weights of the filter are studied. Using the optimum clock waveforms suggested for driving tapped and untapped CCD delay lines, an appreciable enhancement in the charge transfer efficiency and dynamic range of these devices has been achieved and the results are reported in the thesis.

CONTENTS