CERTAIN INVESTIGATIONS ON IMPEDANCE SOURCE INVERTERS

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CERTIFICATE

This is to certify that the thesis entitled "**CERTAIN INVESTIGATIONS ON IMPEDANCE SOURCE INVERTERS**" being submitted by **Mr. Chandra Shekar Thelukuntla** for the award of degree of **Doctor of Philosophy** is a record of a bonafide research work carried out by him in the Department of Electrical Engineering of Indian Institute of Technology Delhi, New Delhi. Mr. Chandra Shekar Thelukuntla, worked under my guidance and supervision and has fulfilled the requirement for the submission of the thesis, which to my knowledge has reached the requisite standards. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any Degree or Diploma.

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ABSTRACT

Multi-stage power processing is widely used in dc-ac conversion. However, to achieve higher efficiencies, reduction in number of stages as well as switching devices is desirable. In this context, single-stage dc-ac inverters are better from the efficiency point of view. Moreover, single-stage power conversion topologies require lesser number of control-loops that are sufficient to ensure stable and reliable power conversion. On account of lesser control-loops the degree of freedom is reduced, from control point of view, and imposes duty ratio limitations. Its impact can easily be minimized through an appropriate controller structure, where-in the control-loops has to act in such a way to give optimal pulse width pattern to the single-stage inverter. Therefore, investigations in this thesis are mainly targeted to address the following issues of impedance source inverters: (i) modeling and analysis of impedance source inverters: (a) Z-source inverter, (b) Quasi Z-source inverters, and (c) X-source inverter. (ii) design and optimization of controllers to ensure dc and ac side regulation, (iii) Direct and indirect control of dc-link voltage in the impedance source inverters, (iv) Control of Z-source inverter with constant, adaptive shoot-through duty ratio and modulation indices.

The present work focuses on single-phase single-stage inverter topologies, that are formed by cascade connection of impedance source network with H-bridge inverter. These topologies have embedded buck-boost feature, ease of control, and fewer number of switching devices. The boosting of the dc-link voltage in such topologies is achieved through the impedance source network by controlling the duty ratio termed as shoot-through duty ratio (STDR). This STDR is integrated within the zero state of

inverter switching cycle and does not affect the volt-sec balance of the downstream inverter. Since, the modulation index corresponding to the inverter load voltage unaltered the dc-link voltage; boost control is independent of pulse width modulation associated with the ac-side load voltage regulation. However, at each operating point the sum of shoot-through duty ratio, required for boost control, and the duty ratio determined by the modulation index for load voltage regulation should be maintained constant. Exhaustive investigations on control of Z-source inverters with constant shoot-through duty ratio and modulation index limits are made and in certain cases the Z-source inverter found to be working with saturated limits of duty ratios leading to either insufficient boosting or ac load voltage droop or distortion. In order to overcome these limitations, an algorithm is proposed in this thesis for adaptive selection of saturation limits. Its effectiveness is demonstrated through simulation studies and then prototype experimental measurements.

Although, impedance source topologies belong to single stage conversion systems, but they need suitable controllers to: (i) meet load demand, (ii) handle source and load side variations, (iii) achieve better regulation, and (iv) yield reliable and stable power processing. The reliability of impedance source inverters not only depends on its steady-state design but depends on the controller design as well. In this direction, this thesis makes an attempt to design control schemes ensuring the above stated requirements. Mathematical models of impedance source inverters are formulated through signal flow-graphs. A proportional plus resonant controller is designed to attain the ac load voltage regulation. A design procedure is established to identify all possible proportional plus integral controller parameters to directly control the dc-link voltage. Since, the dc-link voltage in impedance source topologies is of

pulsating nature an appropriate sensing scheme is required. To avoid these limitations, due to the sensing, an indirect dc-link voltage control through Z-source capacitor voltage regulation is proposed. Although, the capacitor voltage sensing is not a difficult task but the simple proportional plus integral controller, used in direct dc-link voltage, is not suitable on account of control-to-Z-source capacitor transfer function. In order to achieve Z-source capacitor voltage control, a proportional plus integral plus derivative controller structure is proposed in this thesis. Stabilizing regions of the three controller parameters (k_p, k_i, and k_d) are generated by solving a set on non-linear inequality equations, after enforcing Hermite-Biehler theorem satisfying the interlacing property. An important property of these regions is that all admissible controller combinations, easily identifiable without needing trial and error tuning, ensures closed-loop system stability and also closely satisfies the design specifications. A manual selection of optimal and yet feasible controller parameters from these stabilizing regions is a challenging task. In view of this, a particle swam optimization based search technique is used in this thesis to identify the optimal controller parameters, from the known stabilising regions, based on the minimisation of integral time absolute error (ITAE) performance index subject to the relative stability constraints. The developed models are used in design of controllers and their feasibility is demonstrated on a Z-source inverter to ensure dc and ac side regulation. The theoretical predictions have been validated through experimental investigations.

Contents

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS AND ABBREVIATIONS

$G_{pid}(s)$	PID controller transfer function
$H_z(s)$	Sensor gain transfer function
$G^t_{v_o d_m - o-I}(s)$	terminated Control-to-load voltage transfer function
$G^u_{v_{dclink} d_s - o-Z}(s)$	Unterminated Control-to-dc-link voltage transfer function
$G^u_{v_c d_s}(s)$	Unterminated Control-to-Z-source capacitor voltage transfer function
AST	Active-state
DCLV	DC-link voltage
DDCL	Direct dc-link voltage
DG	Distributed Generation
D_s	Shoot-through duty ratio
EMI	Electromagnetic interference
f_s	Switching frequency
GM	Gain margin
IDCL	Indirect dc-link voltage
I_{dclink}	DC-link current
i_L	Instantaneous inductor current
I_L	Average Inductor current
i_o	Instantaneous load current
I_o	Load current
ITAE	Integral time absolute error
m	Modulation Index
MI	Modulation index
MRPWM	Modified reference Pulse width modulation
NST	Non Shoot-through state
PI controller	Proportional plus integral controller
PID controller	Proportional plus integral plus derivative controller
PM	Phase margin

PR controller	Proportional plus resonant controller
PSO	Particle Swarm Optimization
QZCIC	Quasi Z-source inverter with continuous input current
QZDIC	Quasi Z-source inverter with discontinuous input current
r_1/r_2	Inductor-1, 2 dc resistance
r_{c1}/r_{c2}	Capacitor-1, 2 equivalent series resistance
RHPZ	Right half s-plane zero
SFG	Signal flow graph
SPWM	Sinusoidal Pulse width modulation
ST	Shoot-through state
STDR	Shoot-through duty ratio
SVPWM	Space Vector Pulse Width Modulation
THD	Total harmonic distortion
T_s	One switching time period
V_o	Load voltage
V_c	Average Capacitor Voltage
v_C	Instantaneous capacitor voltage
V_{dc}	Source voltage
V_{dclink}	DC-link Voltage
$v_{L1}/\ v_{L2}$	Voltage across inductor-1, 2
$v_{c1}/\ v_{c2}$	Voltage across capacitor-1, 2
v_o	Instantaneous load voltage
XSI	X-Source Inverter
ZCV	Z-Source Capacitor voltage
ZS	Zero-state
ZSI	Z-Source Inverter
Δv_c	Peak-to-peak capacitor voltage ripple
Δi_L	Peak-to-peak inductor current ripple
ζ	Damping factor
ω_o	Inverter output voltage frequency in rad/sec