

A LOW POWER DESIGN METHODOLOGY FOR TURBO
ENCODER AND DECODER

by

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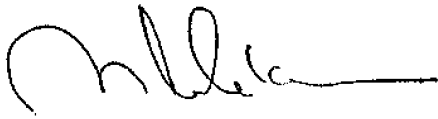
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Certificate

This is to certify that the thesis titled "A Low Power Design Methodology for Turbo Encoder and Decoder" being submitted by Rajeshwari M. Banakar in the Department of Electrical Engineering, Indian Institute of Technology, Delhi, for the award of the degree of Doctor of Philosophy, is a record of bona-fide research work carried out by her under our guidance and supervision. In our opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

The results contained in this thesis have not been submitted to any other university or institute for the award of any degree or diploma.



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Abstract

The focus of this work is towards developing an application specific design methodology for low power solutions. The methodology starts from high level models which can be used for software solution and proceeds towards high performance hardware solutions. Turbo encoder/decoder, a key component of the emerging 3G mobile communication is used as our case study. The application performance measure, namely bit-error rate (BER) is used as a design constraint while optimizing for power and/or area.

The methodology starts from algorithmic level, concentrating on the functional correctness rather than on implementation architecture. The effect on performance due to variation in parameters like frame length, number of iterations, type of encoding scheme and type of the interleaver in the presence of additive white Gaussian noise is studied with the floating point C model. In order to obtain the effect of quantization and word length variation, a fixed point model of the application is also developed.

First, we conducted a motivational study on some benchmarks from DSP domain to evaluate the benefit of custom memory architecture like the scratch pad memory (SPM). The results indicate that SPM is energy efficient solution when compared to conventional cache as on-chip memory. Motivated by this we have developed a framework to study the benefits of adding small SPM to the on-chip cache. To illustrate our methodology we have used ARM7TDMI as the target processor. In this application cache size of 2k or 4k combined with a SPM of size 8k is shown to be optimal. Incorporating SPM results in an energy improvement of 51.3%.

Data access pattern analysis is performed to see whether specific storage modules like

FIFO/LIFO can be used. We identify FIFO/LIFO to be an appropriate choice due to the regular access pattern. A System C model of the application is developed starting from the C model used for software. The functional correctness of SystemC model is verified by generating a test bench using the same inputs and intermediate results used in the C model. One of the computation unit, namely the backward metric computation unit is modified to reduce the memory accesses.

The HDL design of the 3GPP turbo encoder and decoder is used to perform bit-width optimization. Effect of bit width optimization on power and area is observed. This is achieved without unduly compromising on BER. Overall area and power reduction achieved in one decoder due to bit width optimization is 46% and 35.6% respectively.

At the system level, power optimization can be done using power shut-down of unused modules. This is based on the timing details of the turbo decoder in the VHDL model. To achieve this a power manager is proposed. The average power saving obtained is around 55.5% for the 3GPP turbo decoder.

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