TUNNEL FIELD EFFECT AND JUNCTIONLESS FIELD EFFECT TRANSISTORS: INVESTIGATION AND ANALYSIS

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by

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Dedicated to

My Father

Certificate

This is to certify that the thesis entitled "***Tunnel Field Effect and Junctionless Field Effect Transistors: Investigation and Analysis*** " being submitted by **Ms. Sindhu R** for the award of the degree of **Doctor of Philosophy** in the Department of Electrical Engineering, **Indian Institute of Technology Delhi** is a record of bonafide work done by her under my supervision and guidance. The matter embodied in this thesis has not been submitted to any other University or Institute for the award of any degree or diploma to the best of my knowledge.

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Abstract

Small subthreshold swing devices such as Tunnel Field Effect Transistor (TFET) and IMOS Impact Ionization MOS (IMOS) are being widely studied to overcome the limitations such as drain induced barrier lowering, threshold voltage roll off at sub-50 nm channel lengths, and undesirably high static power consumption present in scaled down CMOS devices. However, controlling the gradient of junctions present in these devices in sub-30 nm channel length is a technological problem which demands complicated low thermal budget processes. To overcome this issue, junctionless FETs, which are uniformly and heavily doped, are also being studied widely for scalability. To sidestep the issues present in doped devices due to random dopant fluctuations, the idea of dopingless devices is an emerging area of research with much promise.

An attempt has been made in this work to combine the technological and physical advantages of the idea of dopingless devices with the performance benefits of TFET, IMOS and junctionless devices. The thesis also focusses on an insight into the electrical and physical characteristics of these devices for improving their performance. These devices, made using the charge plasma concept are studied with the help of 2D Technology Computer Aided Design (TCAD) simulations.

A detailed study of the structure and the electrical properties of the TFET made using the charge plasma concept are presented. A method to reduce the ambipolar conduction of the dopingless TFET is also discussed. The fabrication steps for making the dopingless TFET using thin source and drain regions are also presented. Similarly, we have also studied the Impact Ionization transistor made using the charge plasma concept, including the study of the breakdown voltage and the effect of variation of channel length and intrinsic length on the breakdown voltage of the junctionless IMOS.

Continuing with the study of dopingless devices, a raised source/drain structure of the dopingless Junctionless Accumulation Mode FET (JAM FET) is designed and analyzed in detail, next. A study of the device's parasitic bipolar transistor mechanism and analog performance are also presented. Finally, the thesis proposes and studies a double gate symmetric TFET with n^+ pockets at the source and drain-channel interfaces.

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