FABRICATION AND MODELING OF AUTODOPED BURIED-CHANNEL VMOSTs

By

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DEDICATED

TO

MY PARENTS

CERTIFICATE

This is to certify that the dissertation entitled, "Fabrication and Modeling of Autodoped Buried Channel VMOSTs", which is being submitted by Mr. P. Ratnam to the Indian Institute of Technology, Delhi for the award of the degree of Doctor of Philosophy is a record of bonafide research work carried out by him under our guidance and supervision.

In our opinion this dissertation has reached the standard fulfilling the requirements of the regulations relating in the Degree. The results contained in it have not been submitted in part or in full to any other University or Institute for the award of any degree or diploma.

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ABSTRACT

This thesis is devoted to the fabrication and modeling of Buried Channel MOSFETs useful for high speed circuits. A short channel BCMOSFET structure using V-groove technology is fabricated, using a new process technique called 'autodoping'. The process technique being new, the process controllability and the characteristics of autodoped layers are investigated further. The doping profiles of autodoped layers are measured using a modified C-V technique meant for small area devices. This technique enables to eliminate the large overlap capacitances as compared to the intrinsic gate capacitance of short channel BCMOSFETs.

In modeling the BCVMOST, an equivalent planar model is used. Using the box type approximation for the doping profile in the channel region, analytical solutions are obtained for the drain current voltage characteristics. Analysis is made for all the possible modes of operation of both pinch-off and non-pinch-off devices. A new mode of operation called 'punch-through/accumulation' has been identified and the model equations are developed.

Experimental results are obtained on both autodoped VMOST and ion-implanted planar Buried Channel MOSFETs, to check the accuracy of the model. One of the primary concerns is the accuracy of the box type approximation to the non-uniformly doped channel region. A review of various equivalent box approximations available in the literature is carried out.

A new extraction procedure for a 'BEST BOX', approximation is developed using the various modes of operation of the BCMOSFET. This technique being simple, has been implemented for large scale measurements using a desk top computer.

Finally using the best box approach, the analytical I_D-V_D characteristics of planar BCMOSFET as well VMOSFETs are compared with experiments.

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