POWER EFFICIENT ON-CHIP OPTICAL INTERCONNECTS

ELDHOSE PETER

DEPARTMENT OF COMPUTER SCIENCE & ENGINEERING
INDIAN INSTITUTE OF TECHNOLOGY DELHI

JUNE 2016

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by

ELDHOSE PETER

Department of Computer Science and Engineering

Submitted

in fulfillment of the requirements of the degree of Doctor of Philosophy

to the

Indian Institute of Technology Delhi

June 2016

Certificate

This is to certify that the thesis titled **Power Efficient On-Chip Optical Interconnects** being submitted by **Mr. Eldhose Peter** for the award of **Doctor of Philosophy** in Department of Computer Science and Engineering is a record of bona-fide work carried out by him under my guidance and supervision at the Department of Computer Science and Engineering, Indian Institute of Technology Delhi. The work presented in this thesis has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma.

Smruti Ranjan Sarangi
Assistant Professor
Department of Computer Science and Engineering
Indian Institute of Technology Delhi
New Delhi - 110 016

Acknowledgments

Foremost, I would like to express my sincere gratitude to my supervisor Dr. Smruti Ranjan Sarangi for his continuous support and expert guidance during the entire duration of my Ph.D. His valuable suggestions helped to improve the quality of my research manyfold. He was available even at nights to aid me in writing research papers. His efforts to refine my writing skills will be always remembered. Without his unbounded support, I could not have completed this thesis in this short duration of time. I thank him for supporting me in every aspect of my stay at IIT Delhi. I could not have imagined a better mentor for my Ph.D.

I would like to thank all the professors in the CSE department, especially Prof. P. R. Panda, Prof Anshul Kumar Prof Anuj Dhawan and Prof Kolin Paul for offering their technical advice. I would also like to thank Mrs. Vandana Ahluwalia for her help with the lab resources. She made my life easier by acting quickly whenever I faced problems with AC or drinking water.

I thank my grandparents for showering their love and care towards me. I still remember you grandma, giving me your blessings for the last time just before I left to IIT. A single word, thanks is not enough to honour the hard work and sufferings my mummy and pappa had gone through to make me what I am today. I am indebted to my parents for my entire life. Special thanks to my sister and brother in law for their unconditional love. A very special thanks from the bottom of my heart to my love, Kutty for encouraging me and assisting me both personally and academically. I would like to thank rest of my family for their wonderful support. It was you people who gave me strength by your love and care to remain focused at hard times during my stay at IIT Delhi.

I thank all the members of IIT Delhi Malayali association for all the fun filled celebrations. A special thanks to my beloved friends Samsheerali, Deepak, Dileep, Magan, Daniel, Rajeev, Pachu, Safeer and Ajith Sir for making me feel IIT as my second home. I thank Aswin and Davis for helping me personally and professionally. Thanks to the “Chaya” group for the daily chats refreshed me and kept me away from boredom. A special thanks to “Uchakkanji” members Ragi and Jismy for the every day delicious food. I am grateful to my roommates, Arun and Navas for gifting me the memorable moments.

Thanks to my lab mates Raj, Prathmesh, Gayathri, Sandeep and Sharath for inspiring me. I am truly blessed to have these witty yet loving friends that helped me grow personally and professionally.

I would like to thank all who helped me, directly and indirectly, to make my life in IIT Delhi better.

Above all, I would like to thank God for showing light in my path and to hold my hands to keep me steady throughout my journey.

Eldhose Peter

Abstract

As the number of cores on a chip increases, it gets increasingly difficult to design on-chip networks. Large networks necessitate complicated routing protocols, routers with long pipelines, and inordinate delays in transmitting messages. According to the latest ITRS report [1], optical communication will be feasible in future multi-core systems. This will ameliorate a lot of the problems in conventional networks such as high latency and low bandwidth, But, there are a lot of difficulties in implementing on-chip optical interconnects. In this work, we also concern ourselves with static power issues in optical interconnects. This issue has been regarded as the biggest bottleneck in the scalability of such networks.

We start ab initio. We begin by creating a simulation and modeling framework for basic optical components, propose some novel optical components, and later use them to create networks of varying complexities for large multicore processors.

Initially we create a set of optical components known as OptiKit. This is an open source tool kit which can be used to simulate the optical components in RSoft CAD tool. Then we create an optical network using these components. We present fast and dynamic algorithms to create an optical network in bus and tree format. These networks can support on the fly transformations. We improve this proposed network by adding a few more advanced components that can be used to make the network rearrangements quicker. After that we use this network to support fast NUCA communications by leveraging the network to send NUCA and coherence messages. Then we move on to improve the energy consumption by reducing the static power consumption. We achieve this by reconfiguring the network based on network statistics. Finally, we upgrade the network to support a huge system with 1000 nodes. This work considers the on-chip optical network in detail from the basics of optical components to a complex architecture that can support 1000s of nodes.

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