ENERGY ESTIMATION AND MODELING OF LDPC DECODERS

by

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Certificate

This is to certify that the thesis titled **Energy Estimation and Modeling of LDPC Decoders** being submitted by **Lava Bhargava** for the award of **Doctor of Philosophy** in **Electrical Engineering** is a record of bona-fide work carried out by him under our guidance and supervision at the **Electrical Engineering Department, Indian Institute of Technology Delhi**. The work presented in this thesis has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma.

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Abstract

Advances in VLSI technology has made implementation of large systems on a chip possible. Such increased transistor densities operating at very high frequencies leads to very high power densities at the chip level. Further many of these devices are meant for "portable" systems implying energy being sourced from batteries. This has made energy consumption an important design parameter. Thus, it calls for design methodologies which incorporate energy space exploration at every level of abstraction.

A large number of communication systems employ standards which are fast evolving. These standards specify high throughput, low overheads, optimum utilization of channel capacity and support for a variety of bit error rates. Clearly there is a need to use error control codes which can adapt to a wide range of channel conditions. Low density parity check (LDPC) have been adopted in many new standards as they come close to Shannon limit at low SNRs.

LDPC codes are amenable to parallel implementation with decoding complexity which is linear in block length. Further, non-binary LDPC codes as distinct from binary LDPC codes provide very good performance at short and medium block lengths. This motivates us to explore energy efficient hardware implementation of LDPC codes.

This thesis is targeted towards evolving a framework for energy estimation at the algorithmic level. The major motivation is to compare energy efficiency of

various LDPC algorithms. This is achieved by estimating energy based on activity of various individual hardware components. We have carried out implementations of three binary and two non binary algorithms to meet our objectives.

Chapter 1 discusses the motivation for pursuing this problem. There is a need to create a framework which would enable informed decisions regarding energy consumption at higher abstraction level.

In chapter 2 we carry out a survey of techniques for energy estimation at various levels. Models employed at different levels are based on both implementation details as well as input data characteristics available at that level.

Many algorithms have been reported for decoding of LDPC codes. In chapter 3, we have studied and implemented three binary and two non-binary decoding algorithms. Further their BER performance as well as computational complexity has been captured.

One approach to computing energy consumption of algorithms is through using a hardware model as input for power simulator. In chapter 4, VHDL models for fully parallel implementation of three binary and two non-binary algorithms have been built. These models have been synthesized and energy consumption per code word has been estimated. Our results show that log-likelihood is the most energy efficient among the binary algorithms whereas max algorithm outperforms max^* when comparing non-binary algorithms.

In our approach, energy estimation at a higher level of abstraction is based on component energy models built using characteristics of input data streams. In chapter 5, we survey the prior work on component models and follow it up with our model. Our arithmetic component models are based on two parameters; the average Hamming distance and the average bit location of transitions. This approach though simple but in terms of error percentage compares well with models which use many more parameters.

In chapter 6 we present our energy estimation methodology which is based on estimating and summing up the energy consumption of individual components. The component energy itself is estimated using component enegy models created earlier. The input parameters for these models are obtained from the data streams generated by executing the C models. The results show high-fidelity implying they can be used for early stage design space exploration.

Finally in chapter 7 we list specific contributions of this work as well as suggestions for extending this work. Our specific contributions from the thesis include extensive study of LDPC algorithms from the energy consumption point of view as well as a comprehensive approach for energy estimation at algorithmic level.

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