DESIGN, ANALYSIS AND APPLICATIONS OF INTEGER AND NON - INTEGER ORDER DIGITAL INTEGRATORS AND DIFFERENTIATORS

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by

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Dedicated To My Son

Shreyansh

CERTIFICATE

This is to certify that the thesis entitled, "**Design, Analysis and Applications of Integer and Non -Integer Order Digital Integrators and Differentiators**," being submitted by **Ms Madhu Jain** to Indian Institute of Technology Delhi, for the award of the degree of **Doctor of Philosophy** is a record of bonafide research work carried out by her under our guidance and the supervision. In our opinion, the thesis has reached the standards of fulfilling the requirements of the regulations relating to the degree.

The results obtained here in have not been submitted in part or full to any other University or Institute for the award of any degree or diploma.

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MADHU JAIN

ABSTRACT

The investigation in this research work deals with the design, analysis and applications of integer and non-integer or fractional order recursive digital operators (integrators or differentiators). Integrators and differentiators are two most important components of both integer order and fractional order calculus. These operators are the basic parts of many systems like signal processing, control, radar, sonar, communication and medical applications. Integer order operators are useful for those systems which can be modeled using integral calculus. However, for various dynamic systems, integer order operators do not prove adequate to represent the characteristics accurately. For these types of systems, fractional order operators prove more useful as compared to the integer order ones. To effectively analyze complicated systems with fractional elements, it is necessary to develop approximations to the fractional operators using the standard integer order operators.

Main challenge in design of both digital integer order and fractional order integrators and differentiators is to realize ideal magnitude response with linear phase characteristics. Many methods have been developed to design integer and fractional order operators but they are not able to provide the requisite response characteristics. There is still immense scope of improvement in terms of magnitude and phase response.

In this work, an attempt is made to design integer and fractional order operators with magnitude response close to ideal one and linear phase response. New techniques are applied to design a family of integrators up to fourth order. Some of the existing integrators are linearly interpolated to develop a new integrator of third order. Genetic Algorithm (*GA*) optimization is used to develop digital integrators up to third order from a recursive transfer function with unknown coefficients. A hybrid optimization method of minimax and pole zero and constant (*PZC*) optimization is also used to develop integer order digital integrators from a recursive transfer function with unknown coefficients. The minimax

optimization algorithm based method have tendency that the result may be trapped in the local minimum. Therefore, it is worthwhile to further develop an efficient procedure which attempts to locate the global minimum. Here, pole zero and constant (*PZC*) optimization is applied on the result of minimax optimization to improve the performance of designed integrators. For this, constant, zeros and poles of the transfer function are rewritten by adding a variable parameter in each. These parameters are varied within a defined lower and upper bound and their optimum values are calculated. This result in integrators with improved magnitude and phase response compared to minimax optimized integrators. *GA* has an advantage that it can efficiently search large solution spaces due to its parallel structure. However, it suffers from disadvantages of lack of global search ability and premature convergence. The limitation of *GA* is overcome by *PZC* optimization which improves the efficiency of the designed integrators. A half delay is also introduced in the trapezoidal integration rule to design integrators up to fourth order. These new integrators are much more efficient compared to the trapezoidal integrator in terms of magnitude and linear phase response. New integer order differentiators are also obtained by inverting and modifying the transfer function of proposed integrators.

Proposed integer order integrators and differentiators are analyzed in time domain by observing their square and triangular wave responses, respectively. Simulation results show that the proposed operators outperformed the existing ones in time and frequency domain analysis.

Fractional order integrators are designed by applying direct and in direct discretization on some of the existing integer order operators using continued fraction expansion. Integer order operators, designed in this work having excellent performance are chosen for half order integrators design. Their frequency responses are compared and operator producing half order integrator with highest efficiency is selected to design integrators of other fractional powers also. For this, not only continued fraction expansion but other techniques like Taylor series expansion and rational Chebyshev approximation are also used. New fractional order differentiators are also obtained by using the transfer function of proposed fractional order integrators appropriately.

Comparison of the suggested fractional order operators with the existing ones show remarkable improvement in frequency response. Square wave response for integrators and triangular wave response of differentiators are also observed to show their effectiveness.

Applications of proposed integer and fractional order operators for image processing and control are also investigated in this thesis. Proposed integer order differentiators are tested for edge detection. It is found that these perform well for noiseless images. However, for images having strong noise content, their performances gets degraded. Solution is also provided in this work by proposing a new edge detection algorithm based on the combination of fractional order integrators and differentiators. Simulation results show that the proposed algorithm is effective in both noiseless and noisy conditions. Its performance is also better than that of other algorithms for noisy images. The same is successfully implemented on hardware *DSK* TMS320C6713 for non real time images. However, same procedure can be used for real time images also.

Simulation results also show the effectiveness of proposed integer and fractional order Proportional-Integral-Derivative (*PID*) controllers for speed control of *DC* motor with excellent steady state and transient response. The designed *PID* controllers are also implemented using Arduino mega 2560, and it can be seen that their performance validates the results obtained using simulation.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

J	√-1
ω	Angular frequency in radians
ω_m	Angular Velocity
I	Armature Current
L	Armature Inductance
R	Armature Resistance
E	Back emf (Electromotive Force)
e(t)	Control Error, equals to r(t) - y(t)
u(t)	Control signal generated by controller
p_C	Crossover Probability
V	*DC* Source Voltage
K_d	Derivative Gain
τ_e	Electrical Time Constant
T_e	Electrical Torque
k_e	Electromotive Force Constant
D	Fractional Delay
$PI^{\alpha}D^{\beta}$	Fractional Order Controller
${}_{a}D_{t}^{\alpha}$	Fractional Order Operator, *a* and t are limits and α is the order of operation
k_f	Friction Constant
$\Gamma(x)$	Gamma Function of x
Gx, Gy	Gradients
$\tau_g(\omega)$	Group delay
$(s)^{\pm\alpha}$	Ideal fractional order differintegrator

$(s)^{\pm 1}$	Ideal integer order differintegrator
K_i	Integral Gain
γ	Interpolation Ratio ($0 < \gamma < 1$)
C_L	Length of the chromosome
T_L	Mechanical Load
τ_m	Mechanical Time Constant
J	Moment of Inertia
y(t)	Motor Output
p_M	Mutation Probability
N	Order of the integrator
P	Population Size
K_p	Proportional Gain
R	Radius of unstable pole in any transfer function
r(t)	Reference/ Set point
T	Sampling Period
k_t	Torque Constant
μ	Value of maximum *PARE*

LIST OF ABBREVIATIONS

ASP	Analog signal processing
A/D	Analog to Digital
CCS	Code Composer Studio
CFE	Continued Fraction Expansion
CPLD	Complex Programmable Logic Device
DSP	Digital signal processing
DSPs	Digital Signal Processors
D/A	Digital to Analog
DC	Direct Current
DSK	DSP Starter Kit
DIP	Dual in - Line Package
DRAM	Dynamic Random Access Memory
ECG	Electrocardiogram
EEG	Electroencephalogram
EMF	Electromotive Force
FIR	Finite Impulse Response
FODs	Fractional Order Differentiators
FODIs	Fractional Order Differintegrators
FOIs	Fractional Order Integrators
GA	Genetic Algorithm
HODs	Half Order Differentiators
HODIs	Half Order Differintegrators
HOIs	Half Order Integrators
IIR	Infinite Impulse Response

ITAE	Integral of the Time Absolute Error
IP	Integral – Proportional
ICs	Integrated Circuits
IDE	Integrated Development Environment
JTAG	Joint Test Action Group
LT	Laplace Transform
LOG	Laplacian of Gaussian
LEDs	Light Emitting Diodes
MO	Minimax Optimization
NI	National Instruments
PARE	Percentage Absolute Relative Error
PIC	Peripheral Interface Controller
PZC	Pole, Zero & Constant
P	Proportional
PI	Proportional – Integral
PID	Proportional - Integral – Derivative
RCA	Rational Chebyshev Approximation
RTDX	Real Time Data Exchange
RMSE	Root Mean Square Error
SNR	Signal to Noise Ratio
TSE	Taylor’s Series Expansion
TI	Texas Instruments
USB	Universal Serial Bus