# A FEW PERFORMANCE-ENHANCEMENT TECHNIQUES FOR LSI COMPATIBLE ANALOG MOS CIRCUITS

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## CERTIFICATE

This is to certify that the dissertation entitled 'A Few Perfomance-Enhancement Techniques for LSI Compatible Analog MOS Circuits,' which is being submitted by Mr. Sudhir Aggarwal to the Indian Institute of Technology, Delhi, is a record of the bonafide research work carried out by him under our guidance and supervision.

In our opinion, this dissertation has reached the standard fulfilling the requirements of all the regulations relating to the degree. The results contained in it have not been submitted in part or in full to any other university or institute for the award of any degree or diploma.

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# ABSTRACT

Miniaturisation in various automative, consumer and industrial applications calls for 'on-chip' processing of real-world analog input and output signals. The cost-benefits of large scale integration of digital circuits in MOS technology emphasize the need for implementing analog functions also in MOS technology.

In the present work, a few techniques for the improvement in the performance of analog MOS LSI circuits, especially for CMOS operational amplifiers, have been presented. The potential of MOS transistors has been critically evaluated for analog applications with reference to bipolar transistors which are well established in linear/analog circuits. The relevant analog parameters such as transconductance, output conductance, intrinsic voltage gain and inherent noise etc have been compared for both MOS and bipolar transistors having identical chip areas.

The proposed work endeavours to explore the scope of performance-enhancement of analog MOS LSI circuits with respect to (i) matching of MOS transistors, (ii) gain-enhancement in CMOS operational amplifiers and (iii) variability analysis and yield improvement.

Matched pairs of transistors are of critical importance in analog MOS LSI chips since for many circuits the important performance parameters are a function of the degree of matching available between the transistors. A novel two-dimensional MOS transistor has been proposed which can be used as a matched pair of transistors. The device characteristics in the linear region

have been modeled by solving 2-D current continuity equation. For the saturation region, an empirical relation has been worked out. A test-chip containing the new 2-D MOS transistor has been designed and fabricated. The I-V characteristics for the 2-D MOS transistor have been measured. A basic small-signal equivalent circuit for the 2-D MOS transistor has been proposed. The use of the device in the matched current mirrors and inverting amplifiers has been demonstrated. A few more applications of the device have been envisaged.

To increase the gain of a CMOS operational amplifier, a circuit modification in CMOS differential amplifier has been proposed resulting in a higher gain. The SPICE simulations of the circuit have shown a gain improvement of 16 dB over the conventional cascode differential amplifier. This has been confirmed by the measurements made on the test-chip fabricated with 5-$\mu$m, Si-gate, p-well CMOS technology. Simulations of an operational amplifier using the modified differential input stage show a better performance with respect to the gain, bandwidth, slew-rate and PSRR at high frequencies.

Finally, a technique for variability improvement in MOS LSI circuits has been proposed. A statistical method for predicting the variability has been illustrated with the example of a CMOS operational amplifier. The variability of the gain and the offset voltage of the operational amplifier has been calculated with respect to the variation in threshold voltage. A sensitivity analysis of the gain and offset voltage has been performed with respect to the threshold voltage. A new layout has been proposed for the operational amplifier which results in reduced variability and hence more yield. The statistical data about the threshold voltage variation has been obtained for a 5-μm, Si-gate, p-well CMOS process. The variability of the gain and offset voltage has been found by collecting the data from four wafers of two different runs. The variability of the offset voltage has shown considerable improvement with the proposed layout as compared to the one in which sensitivity considerations were not kept in view.

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