BISIMULATIONS AND PREBISIMULATIONS FOR TIMED AUTOMATA

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DECEMBER 2016

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by

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Submitted

in fulfillment of the requirements of the degree of Doctor of Philosophy

to the

Indian Institute of Technology Delhi
DECEMBER 2016

Certificate

This is to certify that the thesis titled **Bisimulations and Prebisimulations over Timed Automata** being submitted by **Shibashis Guha** for the award of **Doctor of Philosophy** in **Computer Science and Engineering** is a record of bona fide work carried out by him under my guidance and supervision at the **Department of Computer Science and Engineering, Indian Institute of Technology Delhi**. The work presented in this thesis has not been submitted elsewhere, either in part or full, for the award of any other degree or diploma.

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Acknowledgments

Writing the acknowledgement is possibly one of the most challenging tasks since this is the part of the thesis that finds the maximum readership. I take this opportunity to thank my advisor Prof. S. Arun-Kumar who allowed me to pursue my doctoral research under his supervision. It is not only that I learnt various technical skills and subtleties from him but his perspective on research and academia has broadened my horizon and helped me recognize academics and research as a way of life. He has always been very supportive and liberal about letting me choosing my research problems and towards my visits and internships in other institutes and working with other collaborators.

Chinmay Narayan was a good friend since my M.Tech days. We joined the PhD programme in IIT Delhi on the same day. He was always there as a wall, on whom I could bounce my ideas and in return get some excellent feedback. His immaculate style of formalizing things helped me learn a great deal. With him I could possibly talk about anything and everything. I would remember him as someone who would constantly encourage me during those bad days when things appeared to move very slowly and sometimes even refused to make any progress. I would also remember him as a friend who likes singing in a way that warrants that nobody would like to hear him twice.

I thank Prof. Srinath Srinivasa who was my research advisor during my M.Tech at IIIT Bangalore. His students, including me, used to look up to him as a source of inspiration. His constant encouragement towards solving problems introduced me to research and laid the foundation for joining the PhD programme at a later stage.

It was exciting to work with Mihir Mehta on the ReLTS project. I had a wonderful time discussing with him the design and the implementation of the tool. In the verification lab in IIT Delhi, I was fortunate to find Divyanshu with whom I spent hours discussing problems. He had been very helpful in reviewing some of the proofs in this thesis. Also my sincere thanks to Chandrika for giving me valuable feedback while preparing several of my presentations that I made in the course of my PhD.

I am indebted to Prof. Krishna S. of IIT Bombay, who has been very kind to allow me to visit Centre for Formal Design and Verification of Software (CFDVS) at IIT Bombay as and when I wanted to. I also thank Prof. Ashutosh Trivedi of IIT Bomnbay with whom I had several insightful discussions. Many of these discussions with Prof. Krishna S. and Prof. Ashutosh Trivedi introduced me to various interesting research problems and the current research trends that are aligned with my research interests. I must also mention Prof. Supratik Chakraborty's support for arranging my visit to IIT Bombay on the very first occasion. Without that the successive visits would not have been possible.

I thank Dr. Nathalie Betrand and Dr. Frederic Herbreteau for hosting me during my visit to INRIA at Rennes and LaBRI at Bordeaux respectively in France. I had a very fruitful time while working with both of them during that visit.

My sincere thanks to Prof. Sanjiva Prasad, Prof. Astrid Kiehn and Prof. Kolin Paul for agreeing to be in my doctoral research committee and providing me with valuable feedback in the course of my PhD. I also thank Prof. Saroj Kaushik, the head of the Department of Computer Science and Engineering at IIT Delhi for her support towards procuring laptop and other grants that made things easier and free from hassles.

Paper work was made a lot easier by the Department staff: Mrs. Renu Bhatia, Mr. Rathinam, Rekha and Hemant. I also thank Mr. Rajinder of the PG section and Mr. Chopra of the accounts section for facilitating paper work on several occasions. Mr. Chandu and Mr. KK, the CFDVS staff at IIT Bombay have also been very kind in terms of the logistics support that I needed. Further, I thank Microsoft Research India for supporting my PhD work through their generous fellowship.

Life in IIT would have been less fun in the absence of Syamantak's jokes, his compulsive laughs, our news gazette Gayathri, Shashank's recommendation of Mehdi Hassan ghazals and the Martin Scorsese movies and intruding into Anamitra's home and ensuring that he gets enough food for us. I also thank Suvam, Brojeshwar, Nisha, Dipanjan, Anirban, Swati, Manoj, Yamuna, Sharat, Namita, Sayak, Anup, Mona, Rudra, Jatin, Arindam,

Sandeep, Rajshekar, Prathamesh, Madhulika, Aditi and Parul for sharing some of the nice moments that I would cherish for long. At IIT Bombay, Hrishikesh, Ramchandra, Shahajhan, Abhisekh and in France, Paulin, Srinivas, Yogesh and Sagnik were always around whenever there was a need, however small it may be. I thank them all.

Last but not the least, I thank my parents for their enormous support, love and encouragement towards my education and infusing me with all the values, patience and courage that one needs to face various challenges in the journey called life and more specifically in the course of PhD. Their constant endeavour to provide me with the best education had enabled me to enroll in my doctoral studies that culminated in this thesis. I dedicate this thesis to them.

Shibashis Guha

Abstract

Timed automata, introduced in [1] is a popular formalism for modelling and analysing real time systems. During the last two decades, significant progress has been made in both theory and practice on this formalism. Control state reachability in timed automata was proved to be decidable and is PSAPCE-complete [1]. Several tools have been developed for verification of timed automata. Among them UPPAAL [2, 3], KRONOS [4] and CMC [5] are worth mentioning. Several protocols, controllers and real time algorithms have been verified and industrial case studies have been made using these tools [6, 7, 8, 9]. Though timed language equivalence is known to be undecidable for timed automata [1], timed bisimulation equivalence and time abstracted bisimulation equivalence have been proved to be decidable for timed automata [10, 11].

Speed dependent preorders based on bisimulation have been defined in process algebra frameworks to compare the responsiveness of two functionally equivalent systems. A faster than precongruence, based on a timed extension to Milner's Calculus for Communicating Systems (CCS) [12], has been defined in [13]. The relative efficiency of two processes has been defined based on the number of internal actions performed by each of them in the paper [14]. Performance preorders based on durational actions [15, 16] have also been studied in [17].

In this thesis, we define an 'at least as fast as' relation between two timed automata. The relation is based on the notion of bisimulations and prebisimulations. Prebisimulation for timed automata is an unexplored area and to the best of our knowledge, this is the first such instance where decidability of prebisimulation over timed automata is studied. We show the decidability of the timed performance prebisimulation relation for one clock timed automata using a zone graph [18, 19] construction in PTIME. A zone graph induces a coarser abstraction of the state space of the timed automata compared to the more traditional region graph [1] construction. Thus the construction of a zone graph in general leads to a smaller arena for verification and analysis of timed automata.

In the thesis, we show that our construction leads to a unifying approach to decide various equivalence and preorder relations for timed automata. The method also leads to a game characterization of the relations where the game is played on the zone graphs of the two timed automata being compared. The game characterization further produces an infinite game hierarchy that leads to defining an infinite hierarchy of timed relations. Corresponding to the game for timed bisimulation, we also show a method to generate a timed Hennessy-Milner logic [20, 21] based distinguishing formula if the two timed automata are not timed bisimilar.

Checking any timed and time abstracted relation over timed automata, analysis and model checking of timed automata involve construction of a zone graph or the region graph of the timed automata. The size of the zone graph or the region graph is exponential in the number of the clocks of the timed automaton [1]. Hence it is desirable to have a timed automaton with the least possible number of clocks. While the problem of checking whether a timed automaton accepting the same timed language but with fewer clocks exists is known to be undecidable [22], in this thesis, we have described a method, which given a timed automaton A, produces another timed automaton with the smallest number of clocks that is timed bisimilar to A.

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