ESD DEVICE DESIGN AND STRATEGY FOR STATE OF THE ART CMOS TECHNOLOGIES

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ESD DEVICE DESIGN AND STRATEGY FOR STATE OF THE ART CMOS TECHNOLOGIES

by

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CERTIFICATE

This is to certify that the thesis titled **"ESD Device Design and Strategy for State of the Art CMOS Technologies**" submitted by **Radhakrishnan. S** for the award of **Doctor of Philosophy** in Electrical Engineering is a record bonafide work carried out by him under my guidance and supervision at the Department of Electrical Engineering. The work presented in this thesis has not been submitted elsewhere either in part or full, for the award of any other degree or diploma.

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ABSTRACT

Electrostatic discharge (ESD) is a physical phenomenon wherein there is a rapid transfer of charge between two bodies with different electrostatic potential, when they come in contact with one another. Similar events can also happen in semiconductor industry. An independent research suggests more than 50% of the failures in the semiconductor industry are due to electrical overstress and ESD phenomenon. Especially with technology scaling, the ESD design window also shrinks, traditional ways of ESD protection strategy needs to be reviewed. In this work, we have explored innovative ways of using parasitic current paths to reduce the impact of the ESD stress. The organization of this work is as follows,

IMOS based ESD Clamp: In this work, we have investigated the use of controlled impact ionization mechanism in mitigating the ESD stress. The ESD behavior of the partially gated diode often called as impact ionization MOSFET is explained. We have explored its applicability for 5 V ESD protection using thin gate oxide devices (designed to handle 1.8 V – 2.5 V).

TFET based ESD Clamp: In this work, we have investigated the application of band to band tunneling current in discharging the ESD current. The architecture of the tunnel field effect transistor is similar to the gated diode structure but optimized for tunneling. Extensive TCAD simulations using 28 nm FDSOI technologies were performed to understand nature of the ESD behavior of these tunnel field effect transistors. We have performed TLP measurements of the TFET using different configurations on the TFETs fabricated in the FDSOI technology. Impact of tunnel boosters like silicon germanium and structural optimizations like nanowire technology were also studied. A new on-chip ESD protection network is also proposed. We have also explored the applicability of the TFET in the static ESD protection aimed for failsafe and fault tolerant I/O’s.

Low Leakage Power Clamp: In this work, we explore the usage of the parasitic BJT in the RC based power clamp. In the proposed architecture, the gate and substrate are tied together to enhance the current path from MOSFET and BJT action. The proposed architecture reduces the net width of the bigFET thereby reducing the static leakage current and exhibits faster turn-on capability.

सार

इलेक्ट्रोस्टैटिक डिस्चार्ज (ईएसडी) एक भौतिक घटना है जिसमें विभिन्न इलेक्ट्रोस्टैटिक क्षमता वाले दो निकायों के बीच तेजी से हस्तांतरण होता है, जब वे एक दूसरे के संपर्क में आते हैं। अर्धचालक उद्योग में भी ऐसी ही घटनाएँ हो सकती हैं। एक स्वतंत्र शोध से पता चलता है कि अर्धचालक उद्योग में 50% से अधिक विफलताएं विद्युत ओवरस्ट्रेस और ईएसडी घटना के कारण होती हैं। विशेष रूप से प्रौद्योगिकी स्केलिंग के साथ, ESD डिज़ाइन विंडो भी सिकुड़ती है, ESD सुरक्षा रणनीति के पारंपरिक तरीकों की समीक्षा की जानी चाहिए। इस काम में, हमने ईएसडी तनाव के प्रभाव को कम करने के लिए परजीवी विद्युत रास्तों का उपयोग करने के अभिनव तरीकों का पता लगाया है। इस कार्य का संगठन इस प्रकार है,

IMOS आधारित ईएसडी क्लैंप: इस कार्य में, हमने ईएसडी तनाव को कम करने में नियंत्रित प्रभाव आयनीकरण तंत्र के उपयोग की जांच की है। आंशिक रूप से गेट किए गए डायोड के ESD व्यवहार को अक्सर प्रभाव आयनीकरण MOSFET कहा जाता है। हमने पतले गेट ऑक्साइड उपकरणों (1.8 V - 2.5 V को संभालने के लिए डिज़ाइन) का उपयोग करके 5 V ESD सुरक्षा के लिए इसकी प्रयोज्यता का पता लगाया है।

TFET आधारित ईएसडी क्लैंप: इस कार्य में, हमने ईएसडी करंट के निर्वहन में बैंड टू बैंड टनलिंग करंट के अनुप्रयोग की जांच की है। सुरंग क्षेत्र प्रभाव ट्रांजिस्टर की वास्तुकला गेटेड डायोड संरचना के समान है लेकिन सुरंग के लिए अनुकूलित है। 28 एनएम एफडीएसओआई तकनीकों का उपयोग करते हुए व्यापक TCAD सिमुलेशन इन tunneling ट्रांजिस्टर के ईएसडी व्यवहार की प्रकृति को समझने के लिए किया गया था। हमने FDSOI तकनीक में गढ़े TFETs पर विभिन्न विन्यासों का उपयोग करके TFET की TLP माप का प्रदर्शन किया है। टनल बूस्टर के प्रभाव जैसे सिलिकॉन जर्मेनियम और संरचनात्मक अनुकूलन जैसे नैनोवायर तकनीक का भी अध्ययन किया गया। एक नया ऑन-चिप ईएसडी सुरक्षा नेटवर्क भी प्रस्तावित है। हमने ईएसडी सुरक्षा में सफल और fault tolerant I / O के उद्देश्य से TFET की प्रयोज्यता का पता लगाया है।

कम रिसाव पावर क्लैंप: इस कार्य में, हम आरसी आधारित पावर क्लैंप में परजीवी BJT के उपयोग का पता लगाते हैं। प्रस्तावित वास्तुकला में, MOSFET और BJT कार्रवाई से वर्तमान पथ को बढ़ाने के लिए गेट और सब्सट्रेट को एक साथ बांधा गया है। प्रस्तावित वास्तुकला

बिगफेट की शुद्ध चौड़ाई को कम कर देता है जिससे स्थैतिक रिसाव की धारा कम हो जाती है और तेजी से चालू क्षमता प्रदर्शित होती है।

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