

VLSI DESIGN PROCESSES: MODELING AND IMPROVEMENT

by

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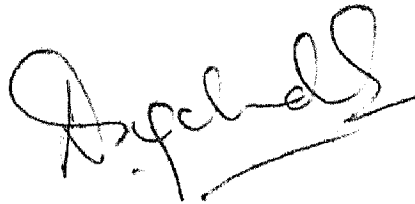
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*This thesis is dedicated to
My Teachers,
My late grand-mother and
My parents and grand-father.*

Certificate


This is to certify that the thesis entitled "*VLSI Design Processes: Modeling and Improvement*", being submitted by **Vineet Sahula** to the Department of Electrical Engineering, Indian Institute of Technology, Delhi, for the award of the degree of Doctor of Philosophy, is a bonafide research work carried out by him under our supervision and guidance. The results obtained in this thesis have not been submitted to any other university or institute for the award of any other Degree or Diploma.



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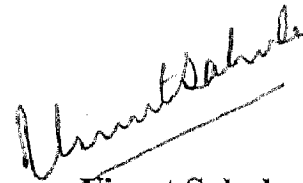
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Abstract

Since the complexity of modern VLSI systems has grown super-exponentially in recent years, the optimization of the design processes for these systems has become vital to achieve lower design cost and shorter time-to-market. Design time forms a major portion of the time-to-market. In fact, design cost is also minimized by reducing design time and development cost. Hence optimization of design time has become a chief concern amongst chip vendors and design houses.

The problem of minimization of design time is complicated by the need for (1) a large number of design iterations, (2) increased interaction between the design levels, (3) communication between large and geographically distributed design teams, and (4) the increasing uncertainty in the convergence of a design process. In this perspective, there is a compelling need to focus on the design processes, analyze them and explore the possibilities of improving them. Estimation of the design completion time is difficult because of the stochastic nature of task completion times and transition probabilities. Various process modeling approaches for estimation of design completion time have been proposed in the past which are capable of modeling only some of the features of a design process. For example, they do not permit hierarchy in the representation of a design process; and stochastic variables cannot be used in place of deterministic values for process model parameters such as task completion times and transition probabilities.

The work, reported in this thesis, is concerned with modeling of VLSI design processes. Our approach, which we call as Hierarchical Concurrent Flow

Graph approach (HCFG), is an analytical approach which allows hierarchical representation of concurrent processes as well as stochastic variations of process parameters. A calibration procedure based on non-linear regression fitting, is proposed for characterization of parameters of HCFG model in terms of design characteristics and designer's characteristics.

The HCFG is supported by a process description language DFLOW, which is a simple textual script capable of describing aforesaid process features. The flow graph to be described in DFLOW, in general may have cycles, AND-concurrency nodes and OR-concurrency nodes.

A detailed decision framework for process improvement using HCFG approach is illustrated. Process completion time minimization has been attempted and achieved by varying process model parameters and exploiting their interrelation. The HCFG modeling and improvement technique has been illustrated in several design flows- (1) ASIC design flow, (2) MCM design flow, (3) design flow for wireless mobile transceiver chip (4) deep submicron physical design flow and (5) software design flow for application specific instruction set processor/DSP. However, the improvement in process completion time is accompanied by increased design effort and decreased resource utilization factor.

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