AN INTEGRATED SOLUTION FOR BUILT-IN SELF TEST

By

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Certificate

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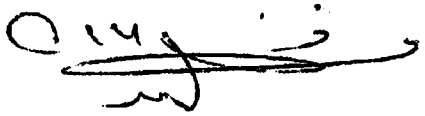

Mohammed Fadle Abdulla

Abstract

Signature based techniques have been well known for the built-in self-test of integrated systems. Conventional BILBO-BIST schemes suffer from long detection latency, since it is not until the signatures are scanned out and compared off-chip that a fault becomes apparent. Aliasing and long test application time, which are fallouts of long detection latency, are serious problems. Other problems of conventional BILBO-BIST are expensive simulations and poor fault diagnosis.

The work reported in this dissertation is concerned with a Built-In Self-Test methodology that can overcome the limitations mentioned above. These test architectures are sufficiently general and applicable to any digital system. We develop improved techniques for improving (a) the probability of aliasing (b) test application time (c) fault simulation time, and (d) fault diagnosis.

In this thesis, we propose two test architectures, called Mulitple On-chip Signature Comparison (MOSC) and Enhanced Mulitple On-chip Signature Comparison (EMOSC), which allow concurrent testing and on-chip signature comparison of multiple intermediate signatures. Data paths can be made testable using a new BIST structure called Concurrent Intermediate Comparison register (CIC). Analysis of the aliasing probability in BILBO as well as in CIC registers using algebraic codes shows the benefit of using these schemes. We have shown that the MOSC and EMOSC techniques are applicable to data paths with embedded memory elements. We have also developed an optimization techniques to reduce the area overhead of the test schemes. Fault simulation and fault diagnosis based on MOSC and EMOSC schemes has also shown good results.

In addition to pure signature based approaches, we describe a novel Mutual Checking BIST architecture (MC-BIST) which uses Equality Comparator register (E-BILBO) to implement mutual testing among functional blocks. We also develop the theory and the design techniques to unify mutual checking with the multiple signature checking schemes.

Keywords : Multiple signature checking, on-chip signature comparison, mutual testing, diagnostic simulation based on multiple signature checking.

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