A MICROPROGRAM GENERATING SYSTEM WITH EMPHASIS ON SIGNAL PROCESSING ARCHITECTURES

BY

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C E R T I F I C A T E

This is to certify that the thesis entitled 'A Microprogram Generating System with Emphasis on Signal Processing Architectures', being submitted by M. BALAKRISHNAN for the award of the degree of Doctor of Philosophy to the Indian Institute of Technology, Delhi, is a record of bonafide research work done by him under our supervision. The results contained therein have not been submitted to any other University or Institute for the award of any degree or diploma .

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A C K N O W L E D G E M E N T

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M. BALA KRISHNAN

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to my parents

A B S T R A C T

Microprogramming as a design philosophy has been widely accepted for implementing the control section of digital systems. Further, microprogramming has always appeared promising with regard to offering a user control on architectures. However, the development of user microprogramming has been limited by support software. This dissertation is an effort in designing a software package to support user microprogram generation.

The utility of the proposed microprogram generating system (called PRAM) is established by considering three different signal processing architectures. Even though we have chosen the area of signal processing, this package is general enough to be useful for designing any digital system. The hardware design process necessarily involves certain amount of backtracking i.e. redesign and modifications at different stages. Many of these changes are bound to affect the microarchitecture of the system. Thus, if the package is to be useful, it should be retargetable.

The three major components of such a microprogram generating system are

i. Microprogramming language and translator.

ii. Microprogram compaction subsystem.

iii. Microcode simulator.

An extensive survey of microprogramming languages is followed by the design of a language for PRAM. The language provides for a unified syntax to describe target microarchitecture as well as the algorithm to be microprogrammed. Some important features of this language are:

i. Data transformations to be specified at register transfer level.

ii. Control flow using PASCAL like branch and loop constructs.

iii. Low level access for directly assigning microorders.

The translator analyses the microarchitecture declarations to generate all feasible register transfer operations. The source algorithm is then mapped on to the microarchitecture to generate a list of microoperations for the compaction process.

The compaction subsystem uses a modified critical path algorithm to generate microcode. The algorithm implemented achieves local compaction i.e. compaction within a straight line segment. But it has the capability to handle branches and loops, and generates branch addresses automatically.

An interactive microprogram simulator featuring logic state analyser like trace facilities has been designed for hardware design evaluation and microcode validation. The target specific simulation routines can be synthesised from the microarchitecture description.

The dissertation establishes the suitability of PRAM for digital hardware design by generating microcode for, example signal processing systems.

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