

**TCAD Based Modelling of Line-Edge-Roughness and  
Radiation Effects in Advanced CMOS Devices**

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**DEPARTMENT OF ELECTRICAL ENGINEERING  
INDIAN INSTITUTE OF TECHNOLOGY DELHI**

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Radiation Effects in Advanced CMOS Devices**

*by*

**CHANDAN KUMAR JHA**

**DEPARTMENT OF ELECTRICAL ENGINEERING**

*Submitted*

**in fulfilment of the requirements of the degree of Doctor of Philosophy**

*to the*



**INDIAN INSTITUTE OF TECHNOLOGY DELHI**

**APRIL 2021**

*Dedicated to my  
Family and Friends for their  
Continuous Support*

# Certificate

This is to certify that the thesis entitled “*TCAD Based Modelling of Line-Edge-Roughness and Radiation Effects in Advanced CMOS Devices*”, being submitted by Mr. *Chandan Kumar Jha* to the Indian Institute of Technology Delhi, is worthy of consideration for the award of the degree of *Doctor of Philosophy* in Department of Electrical Engineering and is a record of the original bonafide research work carried out by him. The results presented in the thesis have not been submitted in part or full, to any other University or Institute for the award of any degree or diploma.

I certify that he has pursued the prescribed course of research.

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*“The Secret of getting ahead is getting started. The secret of getting started is breaking your complex overwhelming tasks into small manageable tasks, and then starting on the first one.”*

**Mark Twain**

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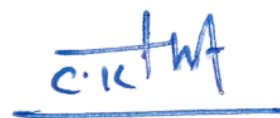
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Chandan Kumar Jha

## Abstract

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CMOS scaling became popular among researchers and the semiconductor industry since it provides many advantages like faster speed, higher performance, and increased integration density on a chip. Despite the above advantages, short channel effects are a major concern for planar devices at lower technology nodes which led to the development of multiple-gate FETs (MugFET), such as Nanosheet FETs (NSFET), Nanowire FET (NWFET), and FinFET as a replacement for planar MOSFETs. Among all these MugFETs, for sub-7nm technology node, NSFETs are a potential replacement of FinFET and NWFETs due to their high drive current and speed. However, the small channel area and doping profile make these MugFETs more susceptible to Process induced variation. In this thesis, some of these issues are discussed and solutions are proposed. The work presented in this thesis is done using Synopsys Sentaurus TCAD and all the characterization is done using Cascade manual prober along with Keysight B1500 parameter analyzer. In the initial part of the thesis, CMOS FETs are designed and simulated using Sentaurus TCAD to match Semiconductor Laboratory (SCL) CMOS 0.18 $\mu$ m device's physical design and electrical characteristics. Id-V<sub>gs</sub> of n and p-type FETs are measured in linear as well as in the saturation region and finally calibrated using the Sentaurus TCAD model. SOI device's faster speed, resistance to latch-up, and immunity against radiation make it preferable over conventional planar devices. PD SOI and FD SOI FETs are also designed to a specific 0.18 $\mu$ m CMOS target using a calibrated TCAD model for radiation analysis.

MugFETs with small channel areas are subject to Line edge roughness (LER) due to process-induced variation. LER can result in a high mismatch in FET's electrical characteristics. In this thesis, a 3-D LER model has been taken for the accurate analysis of mismatch in NS and NW-FETs electrical characteristics.

The mismatch performance of NSFET is investigated and reported for different NS widths. Also, SCE performance parameters, like DIBL (mV) and SS (mV/dec) sensitivity to LER are investigated in this chapter. Moreover, the Junctionless mode devices (JL) are preferred over Inversion mode (IM) devices for nanoscale FETs design due to their simple fabrication process, high drive current, and feasibility of doing short channel length design. However, JL FETs are more susceptible to process-induced variation. This thesis also includes a study of matching the performance of inversion (INV) and junctionless (JL) NS/NW-FETs devices for 3-D LER.

Semiconductor devices are also being widely used in space for various applications, also affected by the presence of Cosmic rays consist of different particles such as heavy-ions, neutrons, protons, electrons, alpha particles, and gamma rays. Among these cosmic ray particles, heavy-ions cause a change in the state of memory element or temporary circuit failure due to instantaneous transient current spike in devices. In the next part of the thesis, heavy-ion induced single event transient (SET) in bulk and SOI NSFET are discussed. Vertically stacked nanosheets are designed and simulated using the inbuilt heavy-ion Sentaurus TCAD model. SET current in bulk and SOI NSFETs for different device dimensions are investigated and discussed in this thesis. Also, the effect of the different angles of ion incidence on SET performance is analyzed. SOI NSFETs show a distinct advantage over bulk devices for heavy-ion SET. Further, different 3-D SOI MugFETs, such as FinFET, NSFET, and NWFET are simulated for SET due to heavy-ion irradiation and compared. Finally, an empirical model is also presented in this thesis to predict the SET current with physical design parameters of MugFETs, and as well as the heavy-ion model parameters. Physical design as well as heavy-ion parameters, such as nanosheet fin width/ thickness, the diameter of a nanowire, linear energy transfer (LET), angle of incidence, and channel doping are incorporated to accurately predict SET due to heavy-ion irradiation on these MugFETs.

## सार

सिमोस स्केलिंग शोधकर्ताओं और सेमीकंडक्टर उद्योग के बीच लोकप्रिय हो गया क्योंकि यह एक चिप पर तेज गति, उच्च प्रदर्शन, और वृद्धि की घनत्व जैसे कई फायदे प्रदान करता है। उपरोक्त फायदे के बावजूद, लघु चैनल प्रभाव लोअर प्रौद्योगिकी नोड्स में पलैनर उपकरणों के लिए एक प्रमुख चिंता का विषय है, जिसके कारण कई गेट वाले फेट्स (मगफेट) का विकास हुआ, जैसे नैनोशीट फेट्स (एन एस फेट), नैनोवायर फेट (एन डब्लु फेट), और फिनफेट के रूप में पलैनर मॉस्फेट्स के लिए एक प्रतिस्थापन। उप-7 एनएम प्रौद्योगिकी नोड के लिए इन सभी मगफेट्स में, एन एस फेट्स अपने उच्च विद्युत धारा और गति के कारण फिनफेट और एन डब्लु फेट्स के संभावित प्रतिस्थापन हैं। हालांकि, छोटे चैनल क्षेत्र और डोपिंग प्रोफाइल इन मगफेट्स को प्रक्रिया प्रेरित भिन्नता के लिए अतिसंवेदनशील बनाते हैं। इस थीसिस में, इनमें से कुछ मुद्दों पर चर्चा की गई है और समाधान प्रस्तावित हैं। इस थीसिस में प्रस्तुत कार्य सिनोप्सिस सेंटोरस टिकैड का उपयोग करके किया गया है और सभी लक्षण वर्णन कैसकेड मैनुअल प्रोबर के साथ किसाइट बी-1500 पैरामीटर विश्लेषक का उपयोग करके किया गया है। थीसिस के प्रारंभिक भाग में, सिमोस फेट को सेमीकंडक्टर प्रयोगशाला (एस सी एल) सिमोस 0.18 माइक्रोन डिवाइस के भौतिक डिज़ाइन और विद्युत विशेषताओं से मेल करने के लिए सेंटोरस टिकैड का उपयोग करके डिज़ाइन और अनुकरण किया जाता है। एन और पि-टाइप फेट के  $I_d-V_{gs}$  को रैखिक के साथ-साथ संतृप्ति क्षेत्र में मापा जाता है और अंत में सेंटोरस टिकैड मॉडल का उपयोग करके कैलिब्रेट किया जाता है। एसओआई डिवाइस की तेज गति, लैच-अप का प्रतिरोध और विकिरण के खिलाफ प्रतिरोधक क्षमता पारंपरिक पलैनर उपकरणों के मुकाबले इसे बेहतर बनाती है। पीडी एसओआई और एफडी एसओआई फेट्स को रेडिएशन विश्लेषण के लिए कैलिब्रेटेड टिकैड मॉडल का उपयोग करके एक विशिष्ट 0.18 माइक्रोन लक्ष्य के लिए डिज़ाइन किया गया है।

छोटे चैनल क्षेत्रों के साथ मगफेट्स प्रक्रिया-प्रेरित भिन्नता के कारण लाइन एन एफनेस (एलईआर) के अधीन हैं। एलईआर फैट की विद्युत विशेषताओं में एक उच्च बेमेल परिणाम कर सकता है। इस थीसिस में, एनएस और एन डब्लु-एफईटी की विद्युत विशेषताओं में बेमेल के सटीक विश्लेषण के लिए 3-डी एलईआर मॉडल लिया गया है।

एन एस फेट के बेमेल प्रदर्शन की जांच और विभिन्न एन एस चौड़ाई के लिए रिपोर्ट की गई है। इसके अलावा, एससीई प्रदर्शन मापदंडों, जैसे डीआईबीएल (mV) और एसएस (mV/dec) एलईआर के प्रति संवेदनशीलता की जांच इस अध्याय में की जाती है। इसके अलावा, उनके सरल निर्माण की प्रक्रिया, हाई ड्राइव करंट और शॉर्ट चैनल लेंथ डिजाइन करने की व्यवहार्यता के कारण, नैनोस्केल एफईटी डिजाइन के लिए जंक्शनलेस मोड डिवाइसेस (जेएल) को इनवर्जन मोड (आईएम) उपकरणों पर पसंद किया जाता है। हालाँकि, जेएल एफईटी प्रक्रिया-प्रेरित भिन्नता के लिए अधिक संवेदनशील हैं। इस थीसिस में 3-डी एलईआर के लिए इनवर्सन (आईएम) और जंक्शनलेस (जेएल) एन एस / एन डब्लु - फैट्स उपकरणों के प्रदर्शन के मिलान का अध्ययन भी शामिल है।

विभिन्न अनुप्रयोगों के लिए अंतरिक्ष में सेमीकंडक्टर उपकरणों का भी व्यापक रूप से उपयोग किया जा रहा है, कॉस्मिक किरणों की उपस्थिति से भी प्रभावित होते हैं जिनमें विभिन्न कणों जैसे भारी-आयन, न्यूट्रॉन, प्रोटॉन, इलेक्ट्रॉन, अल्फा कण और गामा किरण शामिल होते हैं। इन ब्रह्मांडीय किरण कणों के बीच, भारी-आयन उपकरणों में तात्कालिक क्षणिक वर्तमान स्पाइक करंट के कारण स्मृति तत्व या अस्थायी सर्किट विफलता की स्थिति में बदलाव का कारण बनते हैं। थीसिस के अगले भाग में, भारी-आयन प्रेरित एकल घटना क्षणिक (एसईटी) बल्क और एसओआई एन एस फेट में चर्चा की गई है। वर्टिकल स्टैकड नैनोशीट इनबिल्ट हैवी-आयन सेंटरस टिकैड मॉडल का उपयोग करके डिजाइन और सिम्युलेटेड हैं। अलग-अलग उपकरण आयामों के लिए बल्क और एसओआई एन एस फैट्स में एसईटी करंट की जांच की जाती है और इस थीसिस पर चर्चा की जाती है। इसके अलावा, एसईटी प्रदर्शन पर आयन घटना के विभिन्न कोणों के प्रभाव का विश्लेषण किया जाता है। एसओआई एनएसफैट्स भारी-आयन सेट के लिए बल्क उपकरणों

पर एक अलग लाभ दिखाते हैं। इसके अलावा, विभिन्न 3-डी एसओआई मगफेट्स, जैसे कि फिनफैट, एन एस फेट, और एन डब्लु फेट को भारी-आयन विकिरण और तुलना के कारण एसईटी के लिए सिम्युलेटेड किया जाता है। अंत में, एक आनुभविक मॉडल भी इस थीसिस में प्रस्तुत किया गया है ताकि मगफेट के भौतिक डिजाइन मापदंडों और साथ ही हेवी-आयन मॉडल मापदंडों के साथ वर्तमान स्थिति का अनुमान लगाया जा सके। भौतिक डिजाइन के साथ-साथ भारी-आयन पैरामीटर, जैसे नैनोशीट फिन की चौड़ाई / मोटाई, नैनोवायर का व्यास, रैखिक ऊर्जा हस्तांतरण (एलईटी), घटना कोण, और चैनल डोपिंग भारी आयन आयन विकिरण के कारण सही भविष्यवाणी करने के लिए शामिल किए गए हैं इन मगफेट्स पर।

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## LIST OF SYMBOLS

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Symbol	Description
$V_{DD}$	Supply voltage
$V_{DS}$	Drain to source voltage
$V_{GS}$	Gate to source voltage
$V_{ox}$	Voltage across the gate dielectric
$W$	Width of transistor
$L_{ch}$	Gate Channel Length
$I_{ON}$	On Current
$I_{off}$	OFF State Current
$t_{ox}$	Oxide Thickness
$V_{th}$	Threshold Voltage

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## LIST OF ABBREVIATION

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<b>Abbreviation</b>	<b>Description</b>
CMOS	Complementary metal-oxide semiconductor
NSFET	Nanosheet Field Effect Transistor
NWFET	Nanowire Field Effect Transistor
TCAD	Technology Computer Aided Design
SCE	Short Channel Effect
CLM	Channel Length Modulation
DIBL	Drain Induced Barrier Lowering
LET	Linear Energy Transfer
SET	Single Event Transient
LER	Line Edge Roughness
RDF	Random Dopant Fluctuation
MGG	Metal Grain Granularity

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