

**SYNTHESIS OF REGULAR VLSI LAYOUTS
FROM HIGH LEVEL DESCRIPTIONS**

By

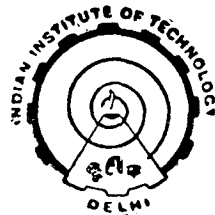
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A Thesis Submitted

In Partial Fulfilment of the Requirements

For the Degree of

DOCTOR OF PHILOSOPHY



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JUNE 1986

CERTIFICATE

This is to certify that the thesis entitled "Synthesis of Regular VLSI Layouts from High Level Descriptions" being submitted by Mr.Kumar Ramayya to the Department of Electrical Engineering, Indian Institute of Technology Delhi for the award of degree of "Doctor of Philosophy" is a record of the bona fide research work carried out by him. Mr.Kumar Ramayya worked under our guidance for the submission of this thesis which to our knowledge has reached the requisite standard.

The thesis or any part thereof has not been submitted to any other university/institution for the award of any degree or diploma.

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ACKNOWLEDGEMENTS

I am extremely grateful to my guides Dr. Anshul Kumar and Prof. Surendra Prasad for the constant guidance and moral encouragement that I received from them. This thesis would not have been possible without their help and guidance.

I thank all my colleagues for the co-operation which they had extended during this period. I thank Shashi Kumar, B.N.S. Murthy, M. Zubair, S.N. Gupta and G.S. Visweswaran for the useful discussions that I had with them.

I thank R. Kapoor, M.S. Sodhi, Pande and M/s. Zerox and Books for helping me with the production of this thesis.

Finally, I thank my family and friends for having stood by me during this arduous task.

Kumar Ramayya

ABSTRACT

This thesis outlines a methodology for synthesizing regular VLSI layouts from high level digital system descriptions. Most existing synthesis methodologies either perform a purely logical synthesis followed by usual placement and routing, or use very restrictive structures to obtain a layout. The design methodology outlined by us considers the topology of the layout at an early stage of design, by using very general structures which are pieced together to generate the overall floorplan. The synthesis of a digital system has been broken up into the synthesis of the constituent control and data parts. Some new structures have been proposed and some existing structures have been used for the hierarchical realization of the control and data parts.

The control part is synthesized from petri-net-like representations (R-Net) which can be easily obtained from high level procedural descriptions. We have proposed a structure called R-Net array (RNA) which can be used to directly map an R-Net description. Another technique for realizing R-Nets that has been discussed in this thesis, uses an interconnection of PLAs. A third methodology for R-Net synthesis replicates the topology of the R-Nets and is called the direct synthesis technique.

Some of the existing data part structures have been examined and their positive features have been extracted and embodied in a new flexible structure called data node array (DNA). Some algorithms have been discussed for realizing a DNA structure from high level structural input descriptions.

The data and control synthesis strategies that have been discussed in this thesis, generate layouts with a variety of shapes which have regular interconnection patterns. A technique for combining these data and control layouts in a hierarchical manner to generate the system layout has also been discussed.

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