

**DESIGN AND ANALYSIS OF 4H-SiC BASED
PLANAR JUNCTIONLESS FETs FOR SUB-10 NM
REGIME**

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DESIGN AND ANALYSIS OF 4H-SiC BASED PLANAR JUNCTIONLESS FETs FOR SUB-10 NM REGIME

by

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*Dedicated to
My family and all the teachers whom I came across at
different stages during my life.*

CERTIFICATE

This is to certify that the thesis entitled "Design and Analysis of 4H-SiC based planar Junctionless FETs for sub-10nm regime" being submitted by **Mr. Jaspreet Singh** for the award of the degree of Doctor of Philosophy in the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under my supervision and guidance. The matter embodied in this thesis has not been submitted for the award of any other degree or diploma.

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Jaspreet Singh

Abstract

The continuous scaling of conventional MOSFETs has reached its limit because of increased short-channel effects (SCE). At ultra-short channel lengths, short-channel effects such as drain induced barrier lowering, threshold voltage roll off, large leakage currents due to its kT/q (where k is the Boltzmann's constant, T is the temperature and q is the electron charge), subthreshold limit, and the need for abrupt doping profiles become a major bottleneck for battery operated devices. If these SCE's are not mitigated properly, they will result in poor switching behaviour of the CMOS transistors. The multiple-gate MOSFETs have provided an alternative to conventional MOSFETs with their enhanced gate control over the channel, thus improving the SCE and the leakage behaviour. However, fabricating abrupt junctions still remains a major concern as it requires high thermal budgets. The introduction of the junctionless FETs (JLFETs) provides a promising solution to this problem.

The JLFETs do not require abrupt junction profiles unlike the conventional MOSFET. In a JLFET, the doping of source, channel, and drain is identical and is of the order of $1 \times 10^{19} \text{ cm}^{-3}$ (for obtaining low source/drain series resistance to realize Ohmic contacts at the source and drain contacts). The JLFETs offer several advantages over conventional MOSFETs, like enhanced immunity over detrimental short channel effects, better scalability, simple fabrication process with reduced thermal budgets and excellent OFF-state characteristics due to volume depletion. The JLFET behaves as a gated resistor, controlled by the applied gate to source voltage. At lower gate voltages, the channel region in a JLFET is fully depleted due to the work function difference between the gate and the channel, as a result the device remains in OFF-state. When the gate voltage is greater than the threshold voltage, the thickness of the depletion region in the channel decreases allowing the current to flow from the drain to the source.

Since, the channel doping is too high, it becomes difficult to achieve volume depletion with gate electrodes of practically realizable work functions (3.9 eV - 5.5 eV). Realizing volume depletion also puts a stringent constraint on the allowed channel thickness for JLFETs. For the efficient depletion of the semiconductor film in the OFF-state, the semiconductor film has to be ultra-thin so that the gate electric field can penetrate and deplete the entire film. Hence, a suitable combination of doping, thickness, and work function of the gate electrode is required while designing JLFETs. Therefore, to achieve efficient volume depletion in JLFETs, various techniques such as high- k dielectric as buried oxide, multi-gate and gate-all-around (GAA) architectures have been experimentally studied. These techniques helped to improve the electrostatic control of gate

over channel. However, the volume depletion of the channel region results in considerable overlap of the conduction band of the drain region with the valence band of the channel region. This band overlap triggers the lateral band-to-band tunneling (L-BTBT) of electrons from the channel region to the drain region in OFF-state ($V_{GS} < V_{Th}$), which is the dominant mechanism for gate induced drain leakage (GIDL) in JLFETs.

The L-BTBT actuates a parasitic bipolar junction transistor (BJT) action in the lateral direction with the hole-rich channel region acting as the P-type base, the N^+ source extension region acting as the emitter and the N^+ drain extension region acting as the collector region. The L-BTBT is quite detrimental to the scaling of the JLFETs and is more pronounced in the efficient gate control architectures. As a result, the NW and NT JLFET architectures suffer from an enhanced parasitic BJT action. The NT JLFET exhibits a larger OFF-state current compared to NW JLFET owing to the presence of the core gate which enhances the LBTBT. The tunnelling current acts as the base current and is amplified by the gain of the parasitic BJT. Thus, the L-BTBT induced BJT action considerably increases the OFF-state current of the NW as well as NT JLFET architectures and hinders their scaling and usage for low power applications. As a result, the JLFETs suffer from a severe degradation in the I_{ON}/I_{OFF} ratio and the proficient gate control in NW and NT architectures is, therefore, not favourable from the perspective of L-BTBT induced GIDL. Thus, L-BTBT needs to be alleviated for the adoption of the emerging FET topologies. Researches have proposed architectures like bulk planar JLFETs, hybrid channel JLFETs and SOI-substrate to mitigate the L-BTBT impact. However, the gain diminishes as the drain-to-source voltage (V_{DS}) is increased. Also, the architectures do not work for channel lengths in sub-10 nm regime. Hence, it becomes even more important and relevant to mitigate the L-BTBT issue for future CMOS scaling.

Therefore, in this doctoral work, various solutions are proposed to mitigate the L-BTBT induced parasitic BJT action and avoid use of complex and costly fabrication architectures like nanowire, gate-all-around and nanotube for sub-10 nm regime. We propose use of P^+ pockets near the source-channel and drain-channel interfaces to realize a planar 4H-SiC JLFETs for sub-10 nm regime. We also show using calibrated device simulations that the 4H-SiC JLFETs exhibit reduced impact of Interface traps unlike conventional 4H-SiC MOSFETs. The proposed 4H-SiC planar JLFETs also exhibit better high-voltage break-down characteristics as compared to conventional Si JLFETs. Moreover, recent studies have shown channel mobility in conventional MOSFETs as high as $\sim 100 \text{ cm}^2/\text{Vs}$, which makes 4H-SiC JLFETs very attractive as a future device for low-power and low-leakage applications, specially the IoT and automotive applications.

We also did a comprehensive analysis of various leakage mechanisms governing the subthreshold performance of sub-10 nm regime 4H-SiC planar JLFETs taking into account (a) Gate induced drain leakage (GIDL) mechanism (b) direct gate tunneling, and (c) inefficient volume depletion. Unlike the silicon-based JLFETs which are significantly impacted by the L-BTBT induced GIDL, the 4H-SiC JLFETs are quite immune to the L-BTBT induced GIDL due to their wider bandgap compared to the silicon. Hence, the leakage mechanism in 4H-SiC can essentially be dictated either by the gate leakage due to the direct tunneling through the thin gate dielectric or the inefficient volume depletion especially for the sub-10 nm regime. Therefore, we have presented the design guidelines for sub-10 nm regime, which can be used for designing required channel length, channel thickness, and gate oxide thickness to have the effective volume depletion.

We have also developed a drain current model for Dual-Material gate JLFET under full and partial depletion conditions using Finite-Differentiation method. We used Finite-Differentiation method to reduce the complex 2-D poisson's equation to simple 1-D poisson's equation, which could potentially help in reducing the significant computational efforts.

सार

शॉर्ट-चैनल प्रभाव (SCE) में वृद्धि के कारण पारंपरिक MOSFETs की निरंतर स्केलिंग अपनी सीमा तक पहुंच गई है। अल्ट्रा-शॉर्ट चैनल लंबाई पर शॉर्ट-चैनल प्रभाव जैसे कि निकासी प्रेरित बाधा कम करना, थ्रेसहोल्ड वोल्टेज रोल ऑफ, इसके kT/q के कारण बड़ी रिसाव धाराएं (जहां k बोल्ट्जमान स्थिर है, T तापमान है और q इलेक्ट्रॉन चार्ज है) सबथ्रेशोल्ड सीमा के कारण डोपिंग प्रोफाइल में तेजी से परिवर्तन की आवश्यकता है। मल्टीपल-गेट MOSFETs ने चैनल पर अपने बढ़े हुए गेट नियंत्रण के साथ पारंपरिक MOSFETs का विकल्प प्रदान किया है, इस प्रकार SCE और रिसाव व्यवहार में सुधार हुआ है। लेकिन तेजी से जंक्शन परिवर्तन बनाना एक प्रमुख चिंता का विषय है क्योंकि इसके लिए उच्च तापीय बजट की आवश्यकता होती है। जंक्शन रहित FETs (JLFETs) की शुरुआत इस समस्या का एक आशा जनक समाधान प्रदान करती है।

JLFET को पारंपरिक MOSFET के विपरीत तेजी से जंक्शन परिवर्तन प्रोफाइल की आवश्यकता नहीं होती है। JLFET में, स्रोत, चैनल और निकासी की डोपिंग समान है और $1 \times 10^{19} \text{ cm}^{-3}$ के क्रम का है। स्रोत और निकासी संपर्कों पर ओमिक संपर्क बनाने के लिए निम्न स्रोत/निकासी श्रृंखला प्रतिरोध को कम करना। JLFETs पारंपरिक MOSFETs पर कई लाभ प्रदान करते हैं, जैसे हानिकारक लघु चैनल प्रभावों पर बढ़ी हुई प्रतिरक्षा, बेहतर मापनीयता, कम थर्मल बजट के साथ सरल निर्माण प्रक्रिया और वाल्यूम डिप्लीशन के कारण उत्कृष्ट ऑफ-स्टेट विशेषताओं। JLFET एक गेटेड रेसिस्टर के रूप में व्यवहार करता है, जिसे एप्लाइड गेट से सोर्स वोल्टेज तक नियंत्रित किया जाता है। लोवर गेट वोल्टेज पर, JLFET में चैनल क्षेत्र गेट और चैनल के बीच कार्य फंक्शन अंतर के कारण बाधित हो जाता है, परिणामस्वरूप डिवाइस ऑफ-स्टेट में रहता है। जब गेट वोल्टेज थ्रेशोल्ड वोल्टेज से अधिक होता है, तो चैनल क्षेत्र में बाधित की मोटाई कम हो जाती है जिससे धारा निकासी से स्रोत तक प्रवाहित हो जाती है।

जब तक, चैनल डोपिंग बहुत अधिक है, व्यावहारिक रूप से प्राप्य कार्य फंक्शन ($3.9 \text{ eV} - 5.5 \text{ eV}$) के गेट इलेक्ट्रोड के साथ वाल्यूम डिफ्लेशन को प्राप्त करना मुश्किल हो जाता है। मात्रा में कमी का एहसास JLFETs के लिए अनुमानित चैनल मोटाई पर एक कठोर बाधा डालता है। ऑफ-स्टेट में सेमीकंडक्टर फिल्म की कुशल वाल्यूम डिफ्लेशन के लिए, सेमीकंडक्टर फिल्म को अल्ट्रा-थिन होना चाहिए ताकि गेट इलेक्ट्रिक फील्ड पूरी फिल्म को बाधित कर सके। इसलिए, JLFETs को डिजाइन करते समय गेट

इलेक्ट्रोड के डोपिंग, मोटाई और कार्य फंक्शन के उपयुक्त संयोजन की आवश्यकता होती है। इस प्रकार से, JLFETs में कुशल मात्रा में कमी को प्राप्त करने के लिए, विभिन्न तकनीकों जैसे कि हाई-के डाइइलेक्ट्रिक जैसे बरी ऑक्साइड, मल्टी-गेट और गेट-ऑल-अराउंड (जीएए) आर्किटेक्चर का प्रयोगात्मक अध्ययन किया गया है। इन तकनीकों ने गेट कंट्रोल ओवर चैनल के इलेक्ट्रोस्टैटिक नियंत्रण को बेहतर बनाने में मदद करती है। हालाँकि, चैनल क्षेत्र के आयतन में कमी के परिणामस्वरूप चैनल क्षेत्र के वैलेंस बैंड के साथ निकासी क्षेत्र के चालन बैंड का काफी ओवरलैप होता है। ऑफ-स्टेट ($V_{GS} < V_{Th}$) में पार्श्व बैंड-टू-बैंड टनलिंग (L-BTBT) ट्रिगर होने पर यह चैनल क्षेत्र से ड्रेन क्षेत्र में इलेक्ट्रॉनों को हस्तांतरित कर देता है। L-BTBT, JLFETs में गेट प्रेरित निकासी रिसाव (जीआईडीएल) प्रमुख यंत्र है।

L-BTBT पार्श्व दिशा में एक आवांछित द्विध्रुवी जंक्शन ट्रांजिस्टर (BJT) क्रिया को क्रियान्वित करता है जिसमें छेद-समृद्ध चैनल क्षेत्र P-प्रकार आधार के रूप में कार्य करता है, N^+ स्रोत विस्तार क्षेत्र उत्सर्जक के रूप में कार्य करता है और N^+ नाली विस्तार क्षेत्र के रूप में कार्य करता है कलेक्टर क्षेत्र में। L-BTBT JLFETs के स्केलिंग के लिए काफी हानिकारक है और कुशल गेट कंट्रोल आर्किटेक्चर में अधिक स्पष्ट है। चैनल पर कुशल गेट नियंत्रण एक उच्च L-BTBT की ओर जाता है और तदनुसार चैनल क्षेत्र में एक उच्च छेद उत्पादन दर को बढ़ा देता है। परिणामस्वरूप, NW और NT JLFET आर्किटेक्चर आवांछित BJT कार्रवाई से अति प्रभावित हो जाते हैं। NT JLFET, NW JLFET की तुलना में एक बड़ा ऑफ-स्टेट करंट प्रदर्शित करता है, जो कोर गेट की उपस्थिति के कारण L-BTBT को बढ़ाता है। टनलिंग करंट, बेस करंट के रूप में कार्य करता है और आवांछित BJT के लाभ से प्रवर्धित होता है। इस प्रकार, L-BTBT प्रेरित BJT कार्रवाई NW के साथ-साथ NT JLFET आर्किटेक्चर के ऑफ-स्टेट करंट को काफी बढ़ा देती है और कम बिजली अनुप्रयोगों के लिए उनके स्केलिंग और उपयोग में बाधा डालती है। परिणामस्वरूप, JLFETs I_{ON}/I_{OFF} अनुपात में एक गंभीर गिरावट से ग्रस्त हैं। NW और NT आर्किटेक्चर में कुशल गेट नियंत्रण, L-BTBT प्रेरित GIDL के दृष्टिकोण से अनुकूल नहीं है। इस प्रकार, उभरते हुए FET टोपोलॉजी को अपनाने के लिए L-BTBT को कम करने की आवश्यकता है। अनुसंधानकर्ता ने L-BTBT प्रभाव को कम करने के लिए बलक प्लेनर JLFETs, हाइब्रिड चैनल JLFETs और SOI-सब्सट्रेट जैसे आर्किटेक्चर प्रस्तावित किए हैं। हालाँकि, ड्रेन-टू-सोर्स वोल्टेज (V_{DS}) बढ़ने पर लाभ कम हो जाता है। इसके अलावा, आर्किटेक्चर sub-10nm regime में चैनल की लंबाई के लिए काम नहीं करते हैं। इसलिए, भविष्य के CMOS स्केलिंग के लिए L-BTBT मुद्दे को कम करना और भी महत्वपूर्ण और प्रासंगिक हो जाता है।

इसलिए इस डॉक्टरेट कार्य में, L-BTBT प्रेरित अवांछित BJT कार्रवाई को कम करने के लिए विभिन्न समाधान प्रस्तावित हैं।

इसलिए इस डॉक्टरेट कार्य में, L-BTBT प्रेरित अवांछित BJT कार्रवाई को कम करने और sub-10nm regime के लिए नैनोवायर, गेट-ऑल-अराउंड और नैनोट्यूब जैसे जटिल और महंगे फैब्रिकेशन आर्किटेक्चर के उपयोग से बचने के लिए विभिन्न समाधान प्रस्तावित किये गये हैं। हम sub-10 nm regime के लिए एक प्लेनर 4H-SiC JLFETs को साकार करने के लिए स्रोत-चैनल और ड्रेन-चैनल इंटरफेस के पास P⁺ पॉकेट के उपयोग का प्रस्ताव करते हैं। हम कैलिब्रेटेड डिवाइस सिमुलेशन का उपयोग करके यह भी दिखा रहे हैं कि 4H-SiC JLFETs पारंपरिक 4H-SiC MOSFETs के विपरीत इंटरफेस ट्रैप के कम प्रभाव को प्रदर्शित करते हैं। प्रस्तावित 4H-SiC प्लेनर JLFETs भी पारंपरिक Si JLFETs की तुलना में बेहतर उच्च-वोल्टेज ब्रेक-डाउन विशेषताओं का प्रदर्शन करते हैं। इसके अलावा, हाल के अध्ययनों ने पारंपरिक MOSFETs $\sim 100 \text{ cm}^2/\text{Vs}$, तक चैनल गतिशीलता को दिखाया है, जो 4H-SiC JLFETs को कम-शक्ति और कम-रिसाव अनुप्रयोगों, विशेष रूप से इंटरनेट ऑफ थिंग्स (IoT) और ऑटोमोटिव अनुप्रयोगों के लिए भविष्य के उपकरण के रूप में बहुत आकर्षक बनाता है।

हमने sub-10nm regime 4H-SiC प्लेनर JLFETs (i) गेट इंड्यूस्ड ड्रेन लीकेज (GIDL) मैकेनिज्म ii) डायरेक्ट गेट टनलिंग, और iii) अकुशल वॉल्यूम रिक्तीकरण के सबथ्रेशोल्ड प्रदर्शन को नियंत्रित करने वाले विभिन्न रिसाव तंत्रों का व्यापक विश्लेषण किया है।)। सिलिकॉन-आधारित JLFETs के विपरीत, जो L-BTBT प्रेरित GIDL से काफी प्रभावित होते हैं, 4H-SiC JLFETs सिलिकॉन की तुलना में अपने व्यापक बैंड गैप के कारण L-BTBT प्रेरित GIDL के लिए काफी प्रतिरक्षित हैं। इसलिए, 4H-SiC में रिसाव तंत्र अनिवार्य रूप से या तो गेट रिसाव द्वारा निर्धारित किया जा सकता है, जो कि पतले गेट डाइलेक्ट्रिक के माध्यम से सीधे टनलिंग के कारण होता है या विशेष रूप से sub-10nm regime के लिए अक्षम मात्रा में कमी के कारण। इसलिए, हमने sub-10nm regime के लिए डिज़ाइन दिशा निर्देश प्रस्तुत किए हैं, जिसका उपयोग आवश्यक चैनल लंबाई, चैनल मोटाई और गेट ऑक्साइड मोटाई को प्रभावी मात्रा में कमी के लिए डिज़ाइन करने के लिए किया जा सकता है।

हमने ड्यूल-मटेरियल गेट JLFETs के लिए पूर्ण और आंशिक कमी की स्थिति में परिमित-भिन्नता पद्धति का उपयोग करते हुए एक ड्रेन करंट मॉडल भी विकसित किया है। हमने जटिल 2-D Poisson's

समीकरण को सरल 1- D Poison's समीकरण को कम करने के लिए परिमित-विभेदन विधि का उपयोग किया है, जो संभावित रूप से महत्वपूर्ण कम्प्यूटेशनल प्रयासों को कम करने में मदद कर सकता है।

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List of Acronyms

IC	Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
IoT	Internet of Things
MOS	Metal Oxide Semiconductor
SCE	Short Channel Effects
SS	Subthreshold Swing
JL	Junctionless
JLFET	Junctionless Field Effect Transistor
FET	Field Effect Transistor
GIDL	Gate Induced Drain Leakage
GAA	Gate all around
BTBT	Band-to-Band Tunneling
L-BTBT	Lateral Band-to-Band Tunneling
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
BJT	Bipolar Junction Transistor
NW	Nanowire
NT	Nanotube
NW JLFET	Nanowire Junctionless Field Effect Transistor
SOI	Silicon on Insulator
SiC	Silicon Carbide
PSG	Phospho-silicate glass
SRH	Shockley-Read-Hall
IalMob	inversion- and accumulation-layer mobility
BV	Breakdown Voltage
DIBL	Drain Induced Barrier Lowering
CPP	Contacted Poly Pitch
BPJLT	Bulk planar Junctionless Transistor
BOX	Buried oxide
DG	Double Gate
T-BTBT	Transverse Band-to-Band-Tunneling
EI	Electrostatic Integrity

EOT	Effective Oxide Thickness
FD	Fully Depleted
UTB	Ultra-thin Body
DMG	Dual Material Gate
DMDG	Dual Material Double Gate
SMG	Single Material Gate
SMDG	Single Material Double Gate
FD	Finite Differentiation
DSDT	Direct Source to Drain Tunneling
TCAD	Technology Computer-Aided Design
SRAM	Static Random-Access Memory
p-JLFET	Junctionless Field Effect Transistor with P ⁺ pocket at both source-channel and drain-channel junctions
sp-JLFET	Junctionless Field Effect Transistor with P ⁺ pocket at drain-channel junctions

List of Symbols

I_{OFF}	OFF-state Current
I_{ON}	ON-State current
I_{ON}/I_{OFF}	ON-state to OFF-state current ratio
C_{dep}	Depletion capacitance of MOSFET
C_{ox}	Gate-Oxide capacitance of MOSFET
V_{Th}	Threshold Voltage
V_{DD}	Supply Voltage
V_{GS}	Gate to Source Voltage
V_{DS}	Drain to Source Voltage
T_{SiC}	SiC channel Thickness
T_{ox}	Gate-Oxide Thickness
N_D	Body Doping Concentration
V_{FB}	Flat Band Voltage
V_{BD}	Breakdown Voltage
L	Gate / Channel Length
2-D	Two Dimensional
1-D	One Dimensional
N_A	P ⁺ Pocket Doping
T_{Ext}	Source / Drain Extension Length
I_{DS}	Drain to Source Current
I_G	Gate Current
WF	Metal-Gate Work Function
L_{el}	Effective Channel Length
x_j	Junction Depth
T_{dep}	Gate Field Penetration Depth
T_{Si}	Silicon Channel Thickness
W	Channel Width
M_1 / M_2	Metal-Gate Work Function
ϵ_{Si}	Permittivity of Silicon
v_T	Thermal Voltage
V	Electron Quasi-Fermi Potential
ϕ_s	Surface Potential

T_{Si}	Si Channel Thickness
Q_{SC}	Space Charge Density
x_d	Depletion Width
Q_d	Fixed Charge Density
R	Effective Channel Resistance
μ_0	Ideal carrier mobility
μ	Carrier mobility
E_c	Critical Electric Field