

THERMAL MODELLING OF MOS INTEGRATED CIRCUITS

by

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*" The sciences of this world are droplets of reality; if they
lead not to reality, what fruit can come of illusion? "*

— from Bahá'í Writings

DEDICATED

**to the Baha'i youth of Iran who have been denied the right
of university education.**

CERTIFICATE

This is to certify that the thesis titled "**Thermal Modelling in MOS Integrated Circuits**" being submitted by Mr. S. M. Noshabadi, for the award of Doctor of Philosophy to the Indian Institute of Technology, Delhi, is a record of bonafide research work he has carried out under our supervision. The results contained in this thesis have not been submitted to any other University or Institute for the award of a degree or diploma.



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" Split the atom's heart , and lo! Within it thou wilt find a sun. "

— Persian mystic poem

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ABSTRACT

With the increasing use of ASIC's, especially in the area of analog and high speed digital VLSI, considerations regarding thermal effects on circuits design and physical placement become more and more important. Thermal effects may represent a limiting factor in the design of IC's. So, with today's level of integration, (VLSI, ULSI and WSI), the need for accurate modelling of thermal behavior of VLSI chip and development of thermal design and placement rules of integrated circuits have become indispensable. This thesis work is devoted to the thermal design and modeling of MOS integrated circuits.

The heat flow problem in the silicon chip has been formulated with the assumption of the MOS device as the basic heat generating source. With this basic formulation, a semi-empirical relation in cylindrical coordinates is derived. This relation is very useful for fast evaluation of temperature maps on the surface of the chip. Some useful results like super-position of temperature profile of several sources, linearity of thermal system have been obtained. The frequency response of the temperature profile is also discussed.

The initial results have been used for the thermal design of the large systems integrated on the chip. We have worked out some simple and convenient thermal placement rules which suit the VLSI environment. These rules state how the heat sources in the circuit should be placed in relation with each other and the other temperature sensitive parts of the circuit, to produce a region of constant temperature, "**Thermal Plateau**". The slope of the temperature profile and its dependence on other parameters of interest has been worked out. It has a very useful application in the design and placement of temperature sensitive blocks. It also discusses how cases of multiple switching and random switching should be managed.

The MOS Transistor circuit has been studied explicitly for thermal effects. The effects of temperature profile, (including Seebeck effect), along the length and the width of the MOS transistors on the I_d and g_m characteristics have been studied. These studies could be important for high precision analog integrated circuits. A SPICE sub-circuit model for MOS transistor, which includes controlled sources to incorporate the static and dynamic temperature variation of the MOS transistor has been developed.

As an example, the circuit design and physical design of a D/A converter has been carried out based on the thermal consideration developed earlier. It is shown how from the statistical distribution of the input pattern the set of critical current sources of the D/A converter are identified, and are placed for the best thermal placement. The thermal sensitivity of a typical CMOS op-amp parameters is performed to help to identify the critical op-amp transistors.