UNIFIED CONTINGENCY RANKING METHODS FOR AC AND AC-DC SYSTEMS

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THESIS SUBMITTED
IN FULFILMENT OF THE REQUIREMENTS FOR
THE AWARD OF THE DEGREE OF

DOCTOR OF PHILOSOPHY

to the

INDIAN INSTITUTE OF TECHNOLOGY, DELHI

INDIA

March, 1990

DEDICATED TO MY BROTHER

PUJYA VIDWAN SHRI MAHANTHA SWAMIGALAVARU

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AND

TO THE LOVING MEMORY OF MY PARENTS

AVVAIAH

APPAJI

CERTIFICATE

This is to certify that the thesis entitled "UNIFIED CONTINGENCY RANKING METHODS FOR AC AND AC-DC SYSTEMS" being submitted by Shri K.L. Putta buddhi for the award of the degree of Doctor of Philosophy, to the Indian Institute of Technology, Delhi, is a record of bonafide research work he has carried out under our guidance and supervision. The results contained in this thesis have not been submitted to any other University or Institute for the award of any degree or diploma.

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ACKNOWLEDGMENTS

I am deeply indebted to my supervisors professor J. Nanda and Dr. P.R. Bijwe for their valuable guidance, encouragement and co-operation during course of my Ph.D. work.

Professor J. Nanda, Dean of U.G. Studies, a luminary in the area of power systems, has been more kind enough in sparing his valuable time and for giving suggestions during this work. His vast research experience, realistic approach have been of great help.

Dr. Bijwe with his brotherly attitude towards me, has been the motive force behind this work. It would have been a difficult task to pursue research after long period of my post graduation but for his untiring pursuasion and exemplary attitude towards academic growth. Dr. Bijwe has been "friend, philosopher and guide" in every sense of the phrase. His invaluable guidance has helped me right from the beginning to the last bit of this work. I consider it my proud previlege to have worked with him. I would ever cherish in my memory the close association and the cardial treatment meted out to me.

I am grateful to professor M.H. Dhanajaya principal. S.J. College of Engineering Mysore for his kind co-operation and encouragement extended towards me.

I have pleasure in expressing my gratitude to my beloved friend and co-research scholar Shri V. BapiRaju who continued to be constant source of inspiration throughout this work.

I am also thankful to my co-research scholars Mr. V. Sankar, Mrs. Mini S. Thomas, Mr. N.D.R. Sarma and K.C. Hari Kumar for their help and co-operation.

This acknowledgement would remain incomplete without expressing my feelings towards my wife Hema, who has been a great source of encouragement. Her invaluable co-operation and sence of understanding will be remembered.

I am grateful to my father-in-law Shri M.N. Puttaswami and mother-in-law M.G. Shankaramma for their parental care shown towards me during this work.

(K.L. PUTTA BHUDDHI)

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ABSTRACT

On-line steady state security analysis of power system requires evaluation of effects of large number of contingency cases to assess the severity. System security assessment is a process whereby any violation of operating limits of power system components is detected. Running an A.C load flow for very large number of cases is tedious, uneconomical and takes prohibitively large computer processing time. Hence, appropriate non-iterative technique have to be employed for real time applications. Contingency ranking methods must satisfy the following four main criteria of goodness (i) less storage (ii) high computational speed (iii) high reliability and (iv) acceptable accuracy as compared to A.C load flow.

From state of art it appears that sufficiently fast and accurate methods for overload contingency ranking are available. However, comparatively lesser number of methods on contingency rankings based on the voltage deviation limit violations are available. Moreover, most of the papers have completely ignored bus type switchings due to reactive power limit violations. To the best of the author's knowledge there are no papers in literature on contingency ranking of A.C system with D.C link. From the view point of computational efficiency unified approaches to

rank the contingencies causing overload and voltage deviations are desirable. Distribution factors are calculated off-line and remain constant as long as network topology is unchanged. Such factors speed up the on-line security analysis tremendously. These are also extremely useful in reducing complexity of security constrained optimization problems. Although, such factors have been developed for overload security, to the best of author's knowledge no such factors are yet available for voltage problem. Keeping this in view unified contingency ranking methods are developed in this work for both A.C and AC-DC systems. Voltage deviation distribution factors for line and generator outages are also developed.

With the above motivation the following methods are developed using current compensations.

(i) Two step compensation method for line outage contingencies using coupled and decoupled Jacobian matrices.

(ii) A single step compensation method for line and generator outage contingencies using coupled and decoupled Jacobian, is developed. VAR limits are checked by using newly developed reactive power shift factors. Voltage distribution factors for simulating outages are also calculated.

(iii) An efficient single step method using coupled and decoupled Jacobians in load flow is developed for systems containing large number of PV buses. Here again voltage distribution factors are calculated. A compensation method for treatment of bus type switching of voltage controlled buses due to reactive power limit violations is also developed.

(iv) For the first time contingency ranking method for A.C system with D.C. link is developed. Using the proposed method line outage distribution factors are calculated.

For all the proposed methods results for overload and voltage deviation rankings have been obtained and compared with corresponding results obtained with rigorous A.C load flow. Results obtained in all cases with proposed methods are in fairly good agreement with those obtained with A.C load flow, although coupled versions have resulted in better ordering accuracy as compared to decoupled versions.