EXPLORING THE RELIABILITY ASPECTS OF NVM TECHNOLOGIES FOR NEUROMORPHIC AND DIGITAL COMPUTING

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by

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DEPARTMENT OF ELECTRICAL ENGINEERING

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Dedicated to

Myself!

“यदा यदा हि धर्मस्य ग्लानिर्भवति भारत।
अभ्युत्थानमधर्मस्य तदात्मानं सृजाम्यहम्।।”

(संदर्भ: श्लोक ७,अध्याय ४, श्रीमद् भगवद् गीता)

हिंदी अनुवाद**:**
हे भारत (अर्जुन)! जब-जब धर्म की हानि और अधर्म की वृद्धि होती है, तब-तब मैं (श्रीकृष्ण) स्वयं को प्रकट करता हूँ।

English Translation:
Hey Arjuna! Whenever there is decline of righteousness, and rise of unrighteousness, then I (Shri Krishna) manifest Myself.

परित्राणाय साधूनां विनाशाय च दुष्कृताम्।
धर्मसंस्थापनार्थाय सम्भवामि युगे युगे।।

(संदर्भ: श्लोक ८,अध्याय ४, श्रीमद् भगवद् गीता)

हिंदी अनुवाद**:**
साधुओं की रक्षा करने के लिए, दुष्कृत्य करने वालों का संहार करने के लिए, धर्म को स्थापित करने के लिए, मैं (श्रीकृष्ण) प्रत्येक युग में प्रकट होता हूँ।।

English Translation:
For the protection of the pious, the destruction of the evil-doers, and establishing virtue, I (Shri Krishna) manifest Myself in every age.

CERTIFICATE

This is to certify that the thesis entitled **“Exploring the Reliability Aspects of NVM Technologies for Neuromorphic and Digital Computing”** being submitted by **Mr. Manoj Kumar** for the award of the degree of Doctor of Philosophy in the Department of Electrical Engineering, Indian Institute of Technology Delhi, is a record of bonafide work done by him under my supervision and guidance. The thesis has reached the standards fulfilling the requirements of the regulations related to the award of the degree. The matter embodied in this thesis has not been submitted for the award of any other degree or diploma.

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New Delhi.

ABSTRACT

Complementary-Metal Oxide Semiconductor (CMOS) technology based classical computing systems (i.e von-Neumann architecture) are energy in-efficient due to physically separated processing and computing units (referred as-memory wall bottleneck), leading to sequential data shuttling between processor and memory. Moreover, going beyond the More-than-Moore's era, deep-sub-micron (DSM) scaling with CMOS technology leads to various challenges such as thermal reliability, high leakage currents, non-uniform features etc. To overcome the aforementioned challenges, exploration of various novel devices and parallel computing principles are much needed.

In this thesis, we explore two emerging Non-Volatile Memory (NVM) technologies i.e Phase-Change Memory (PCM) and Resistive Memory (RRAM) for non-Von-Neumann architecture based Neuromorphic and computational memory applications. We demonstrate exhaustive brain-inspired computing applications through these NVM devices. We emulate the biological synaptic plasticity, dendritic functionality and neuronal activity through the CMOS-NVM based architectures. Moreover to demonstrate the machine learning (ML) based image classification application, we implement the spiking neural networks by incorporating the respective functionalities. Furthermore, through experimental characterizations and CMOS-NVM based circuit simulations, we successfully demonstrate the multi-valued logic and computational memory applications. Various reliability aspects of NVM devices such variability, retention and endurance impacting the proposed brain-mimicking sub-blocks (i.e synapses, dendrites and neurons) and digital logic/memory circuits, are illustrated in this thesis. A detailed benchmarking and comparison with existing studies is also shown to highlight the key advantages (such as area and power) of our proposed implementations.

सारांश

पूरक-धातु ऑक्साइड सेमीकंडक्टर (CMOS) प्रौद्योगिकी आधारित पारंपरिक कंप्यूटिंग सिस्टम (यानी वॉन-न्यूमैन आर्किटेक्चर) भौतिक रूप से अलग प्रसंस्करण और कंप्यूटिंग इकाइयों (जिसे मेमोरी वॉल बॉटलनेक कहा जाता है) के कारण ऊर्जा-कुशल नहीं हैं और इसका मुख्य कारण प्रोसेसर, मेमोरी के बीच सूचना का अनुक्रमिक आदान प्रदान है। इसके अलावा, “मूर” के युग से परे जाकर, डीप-सबमाइक्रोन CMOS तकनीक के साथ स्केलिंग से थर्मल विश्वसनीयता, उच्च रिसाव धाराएँ, गैर-समान विशेषताएँ जैसी विभिन्न चुनौतियाँ सामने आती हैं। उपरोक्त चुनौतियों पर काबू पाने के लिए, विभिन्न नवीन इलेक्ट्रॉनिक कंप्यूटिंग उपकरणों और समानांतर कंप्यूटिंग सिद्धांतों की खोज की बहुत आवश्यकता है।

इस थीसिस में हमने दो उभरती हुई, स्थिर सूचना आधारित मेमोरी (Non-Volatile Memory) तकनीकों, यानी Phase-Change Memory (PCM) और Resistive-Random-Access Memory (RRAM) का उपयोग करते हुए गैर वॉन-न्यूमैन (non Von-Neumann) वास्तुकला आधारित अनुसंधान अनुप्रयोगों, जैसे मानव मस्तिष्क जैसी गणना, कम्प्यूटेशनल मेमोरी की खोज तथा अध्ययन किया है। हमने स्थिर सूचना आधारित मेमोरी तकनीकों के माध्यम से संपूर्ण मस्तिष्क-प्रेरित कंप्यूटिंग सिद्धांतों और अनुप्रयोगों को प्रदर्शित किया है। विशेष रूप से हमने CMOS-NVM आधारित आर्किटेक्चर के माध्यम से मस्तिष्क-प्रेरित जैविक सिनैप्टिक प्लास्टिसिटी, डेंड्राइटिक कार्यक्षमता और न्यूरोनल गतिविधियों को प्रदर्शित किया है। इसके अलावा हमने स्पाइकिंग-न्यूरॉन संबंधित कार्यात्मकताओं को शामिल करके, तंत्रिका नेटवर्क के माध्यम से मशीन लर्निंग (ML) आधारित प्रतिबिंब वर्गीकरण अनुप्रयोगों को प्रदर्शित किया है। आगे, विद्युत प्रयोगों और सर्किट सिमुलेशन के माध्यम से हमने सफलतापूर्वक मल्टी-वैल्यूड-लॉजिक (Multi-Valued-Logic) और कम्प्यूटेशनल मेमोरी जैसे अनुप्रयोगों को प्रदर्शित किया है। स्थिर सूचना आधारित मेमोरी तकनीकों के विभिन्न विश्वसनीयता पहलू, जैसे परिवर्तनशीलता (variability), प्रतिधारण (retention) और सहनशक्ति (endurance) आदि का मस्तिष्क-प्रेरित उप-ब्लॉक (यानी सिनैप्स, डेंड्राइट, न्यूरॉन्स) और डिजिटल लॉजिक/मेमोरी सर्किट पर प्रभाव को इस थीसिस में उद्धृत किया गया है। मौजूदा अध्ययनों के साथ विस्तृत तुलना, हमारे प्रस्तावित कार्यान्वयन और खोजों के प्रमुख लाभों (जैसे क्षेत्रफल और ऊर्जा) को भी इस थीसिस में विस्तार से उजागर किया गया है।

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ABBREVIATIONS

AI	Artificial Intelligence
IoT	Internet of Things
NVM	Non-Volatile Memory
PCM	Phase-Change Memory
OTS	Ovonic-Threshold Switching
NDR	Negative Differential Resistance
CMOS	Complementary-Metal Oxide Semiconductor
LRS	Low Resistance State
HRS	High Resistance State
RRAM	Resistive Random Access Memory
OxRAM	Oxide-based Random Access Memory
DNM	Dendritic Neuron Model
ANN	Artificial Neural Network
AP	Action Potential
PSP	Post-Synaptic-Potential
SNN	Spiking Neural Networks
MNIST	Modified National Institute of Standards and Technology
IMC	In-Memory-Computing
SRDP	Spike Rate Dependent Plasticity
STDP	Spike Time Dependent Plasticity
pMOS	p-type Metal Oxide Semiconductor
nMOS	n-type Metal Oxide Semiconductor
T-Logic	Ternary-Logic
MVL	Multi-Valued Logic
BEOL	Back-End-of-the-Line
NM	Noise Margin
SNM	Static Noise Margin

RNM	Read Noise Margin
WNM	Write Noise Margin
HNM	Hold Noise Margin
SRAM	Static Random-Access Memory
TSRAM	Ternary Static Random-Access Memory
TCAM	Ternary Cintent Addressable Memory